TLA2528 Small, 8-Channel, 12-Bit ADC With I²C Interface and GPIOs

1 Features

- Small package size:
  – 3-mm × 3-mm WQFN
- 8 channels configurable as any combination of:
  – Up to 8 analog inputs, digital inputs, or digital outputs
- GPIOs for I/O expansion:
  – Open-drain, push-pull digital outputs
- Wide operating ranges:
  – AVDD: 2.35 V to 5.5 V
  – DVDD: 1.65 V to 5.5 V
  – –40°C to +85°C temperature range
- I²C interface:
  – Up to 3.4 MHz (high-speed mode)
  – 8 configurable I²C addresses
- Programmable averaging filters:
  – Programmable sample size for averaging
  – Averaging with internal conversions
  – 16-bit resolution for average output

2 Applications

- Mobile robot CPU boards
- Rack servers
- Intra-DC interconnect (metro)

3 Description

The TLA2528 is an easy-to-use, 8-channel, multiplexed, 12-bit, successive approximation register analog-to-digital converter (SAR ADC). The eight channels can be independently configured as either analog inputs, digital inputs, or digital outputs. The device has an internal oscillator for ADC conversion processes.

The TLA2528 communicates via an I²C-compatible interface and supports standard-mode (100 kHz), fast-mode (400 kHz), fast-mode plus (1 MHz), and high-speed mode (3.4 MHz). Up to eight I²C addresses can be selected for the TLA2528 by connecting a resistor on the ADDR pin.

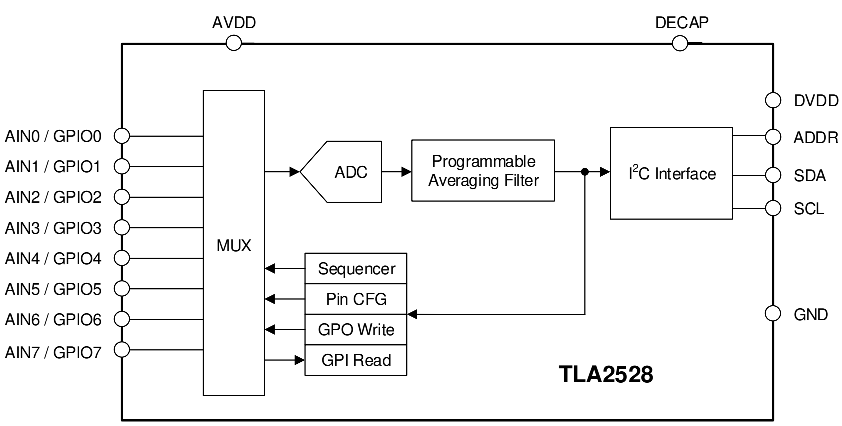
Device Information(1)

PART NAME	PACKAGE	BODY SIZE (NOM)
TLA2528	WQFN (16)	3.00 mm × 3.00 mm

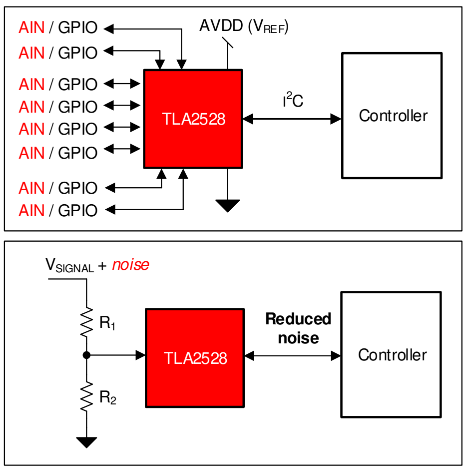
(1) For all available packages, see the orderable addendum at the end of the datasheet.

TLA2528 Block Diagram and Applications

Device Block Diagram



Example Applications



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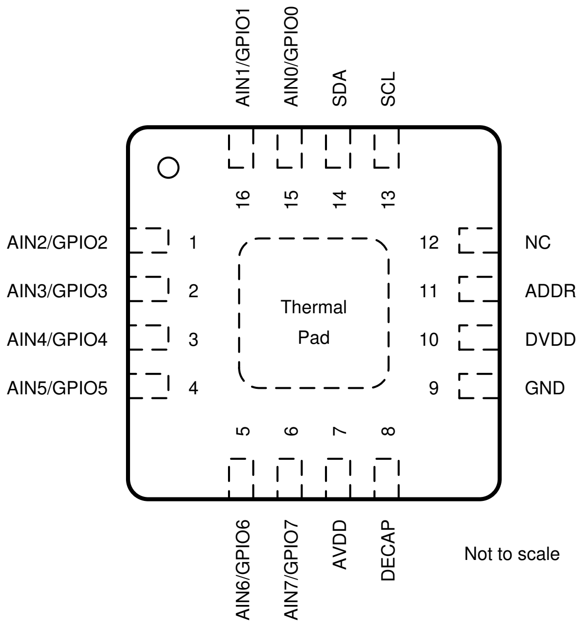
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2019) to Revision A	Page
• Changed document status from advance information to production data	1

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		FUNCTION (1)	DESCRIPTION
NAME	NO.		
AIN0/GPIO0	15	AI, DI, DO	Channel 0; configurable as either an analog input (default) or a general-purpose input/output (GPIO)
AIN1/GPIO1	16	AI, DI, DO	Channel 1; configurable as either an analog input (default) or a GPIO
AIN2/GPIO2	1	AI, DI, DO	Channel 2; configurable as either an analog input (default) or a GPIO
AIN3/GPIO3	2	AI, DI, DO	Channel 3; configurable as either an analog input (default) or a GPIO
AIN4/GPIO4	3	AI, DI, DO	Channel 4; configurable as either an analog input (default) or a GPIO
AIN5/GPIO5	4	AI, DI, DO	Channel 5; configurable as either an analog input (default) or a GPIO
AIN6/GPIO6	5	AI, DI, DO	Channel 6; configurable as either an analog input (default) or a GPIO
AIN7/GPIO7	6	AI, DI, DO	Channel 7; configurable as either an analog input (default) or a GPIO
ADDR	11	AI	Input for selecting the device I^2C address. Connect a resistor to this pin from DECAP pin or GND to select one of the eight addresses.
AVDD	7	Supply	Analog supply input, also used as the reference voltage to the ADC; connect a 1-µF decoupling capacitor to GND
DECAP	8	Supply	Connect a1-µF decoupling capacitor between the DECAP and GND pins for the internal power supply
DVDD	10	Supply	Digital I/O supply voltage; connect a 1-µF decoupling capacitor to GND
GND	9	Supply	Ground for the power supply; all analog and digital signals are referred to this pin voltage
NC	12	No connection	This pin must be left floating with no external connection
SDA	14	DI, DO	Serial data input or output for the I^2C interface
SCL	13	DI	Serial clock for the I^2C interface
Thermal pad	—	Supply	Exposed thermal pad; connect to GND.

(1) AI = analog input, DI = digital input, and DO = digital output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
DVDD to GND	–0.3	5.5	V
AVDD to GND	–0.3	5.5	V
AINx/GPOx(2)	GND – 0.3	AVDD + 0.3	V
ADDR	GND – 0.3	2.1	V
Digital inputs	GND – 0.3	5.5	V
Current through any pin except supply pins(3)	–10	10	mA
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AINx/GPIOx refers to pins 1, 2, 3, 4, 5, 6, 15, and 16.
(3) Pin current must be limited to 10mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		2.35	3.3	5.5	V
DVDD	Digital supply voltage		1.65	3.3	5.5	V
ANALOG INPUTS						
FSR	Full-scale input range	AIN_X(1) - GND	0		AVDD	V
V_{IN}	Absolute input voltage	AIN_X - GND	–0.1		AVDD + 0.1	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	85	℃

(1) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

6.4 Thermal Information

THERMAL METRIC(1)		TLA2528 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_{SH}	Sampling capacitance			12		pF
DC PERFORMANCE						
	Resolution	No missing codes		12		bits
DNL	Differential nonlinearity			±0.45		LSB
INL	Integral nonlinearity			±0.5		LSB
$V_{(OS)}$	Input offset error	Post offset calibration		±0.3		LSB
	Input offset thermal drift	Post offset calibration		±1		ppm/°C
G_E	Gain error			±0.05		%FSR
	Gain error thermal drift			±1		ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	AVDD = 5 V, f_{IN} = 2 kHz		73.2		dB
		AVDD = 3 V, f_{IN} = 2 kHz		72.8		
SNR	Signal to noise ratio	AVDD = 5 V, f_{IN} = 2 kHz		73.3		dB
		AVDD = 3 V, f_{IN} = 2 kHz		73		
DECAP Pin						
C_{DECAP}	Decoupling capacitor on DECAP pin		0.1	1	4.7	µF
	Voltage output on DECAP pin	C_{DECAP} = 1 µF		1.8		V
DIGITAL INPUT/OUTPUT (SCL, SDA)						
V_{IH}	Input high logic level	All I^2C modes	0.7 x DVDD		5.5	V
V_{IL}	Input low logic level	All I^2C modes	–0.3		0.3 x DVDD	V
V_{OL}	Output low logic level	Sink current = 2 mA, DVDD > 2 V	0		0.4	V
		Sink current = 2 mA, DVDD ≤ 2 V	0		0.2 x DVDD	
I_{OL}	Low-level output current (sink)	V_{OL} = 0.4 V, standard and fast mode			3	mA
		V_{OL} = 0.6 V, fast mode			6	
		V_{OL} = 0.4 V, fast mode plus			20	
GPIOs						
V_{IH}	Input high logic level		0.7 x AVDD		AVDD + 0.3	V
V_{IL}	Input low logic level		–0.3		0.3 x AVDD	V
V_{OH}	Output high logic level	GPO_DRIVE_CFG = push-pull, I_{SOURCE} = 2 mA	0.8 x AVDD		AVDD	V
V_{OL}	Output low logic level	I_{SINK} = 2 mA	0		0.2 x AVDD	V
I_{OH}	Output high source current	V_{OH} > 0.7 x AVDD			5	mA
I_{OL}	Output low sink current	V_{OL} < 0.3 x AVDD			5	mA
POWER SUPPLY CURRENTS						
I_{AVDD}	Analog supply current	I^2C high-speed mode, AVDD = 5 V		150	195	µA
		I^2C fast mode plus, AVDD = 5 V		50	75	
		I^2C fast mode, AVDD = 5 V		28	40	
		I^2C standard mode, AVDD = 5 V		12	18	
		No conversion, AVDD = 5 V		7	12	

6.6 I²C Timing Requirements

		MODE(1)				UNIT
		STANDARD, FAST, AND FAST MODE PLUS		HIGH SPEED MODE		
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency(2)		1		3.4	MHz
t_{SUSTA}	START condition setup time for repeated start	260		160		ns
t_{HDSTA}	Start condition hold time	260		160		ns
t_{LOW}	Clock low period	500		160		ns
t_{HIGH}	Clock high period	260		60		ns
t_{SUDAT}	Data in setup time	50		10		ns
t_{HDDAT}	Data in hold time	0		0		ns
t_R	SCL rise time		120		80	ns
t_F	SCL fall time		120		80	ns
t_{SUSTO}	STOP condition hold time	260		60		ns
t_{BUF}	Bus free time before new transmission	500		300		ns

(1) The device supports standard, full-speed, and fast modes by default on power-up. For selecting high-speed mode refer to the section on *Configuring the Device for High-Speed I²C Mode*.
(2) Bus load (C_B) consideration; $C_B \leq 400$ pF for $f_{SCL} \leq 1$ MHz; $C_B < 100$ pF for $f_{SCL} = 3.4$ MHz.

6.7 Timing Requirements

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C.

		MIN	MAX	UNIT
t_{ACQ}	Acquisition time	300		ns

6.8 I²C Switching Characteristics

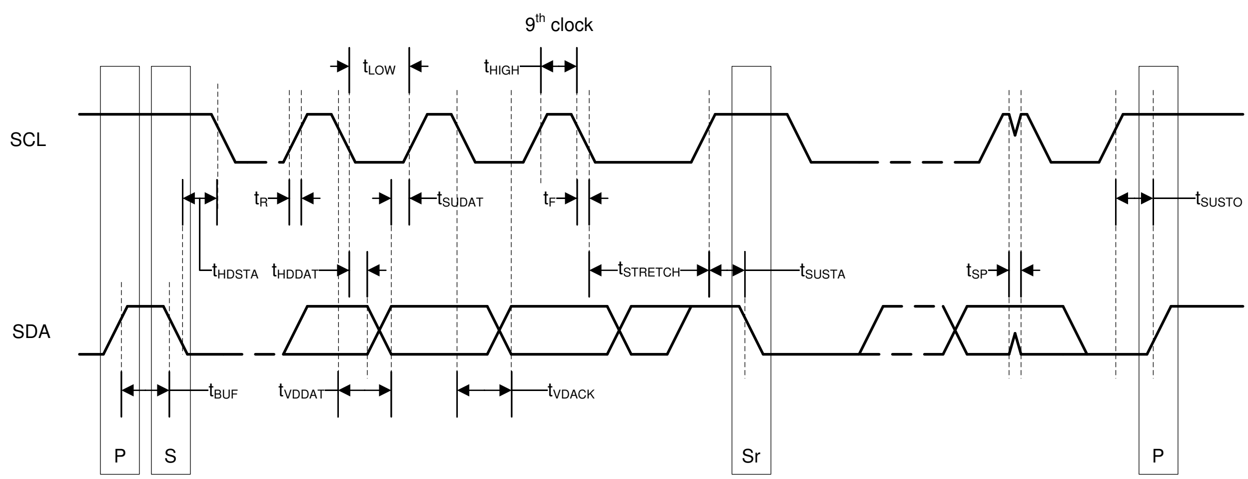
		MODE				UNIT
		STANDARD, FAST, AND FAST MODE PLUS		HIGH-SPEED MODE		
		MIN	MAX	MIN	MAX	
t_{VDDATA}	SCL low to SDA data out valid		450		200	ns
t_{VDACK}	SCL low to SDA acknowledge time		450		200	ns
$t_{STRETCH}$	Clock stretch time in one-shot conversion mode		1400		1000	ns
t_{SP}	Noise supression time constant on SDA and SCL		50		10	ns

6.9 Switching Characteristics

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
CONVERSION CYCLE					
t_{CONV}	ADC conversion time			$t_{STRETCH}$	ns
RESET					
t_{PU}	Power-up time for device	AVDD ≥ 2.35 V		5	ms
t_{RST}	Delay time; RST bit = 1b to device reset complete(1)			5	ms

(1) RST bit is automatically reset to 0b after t_{RST}.

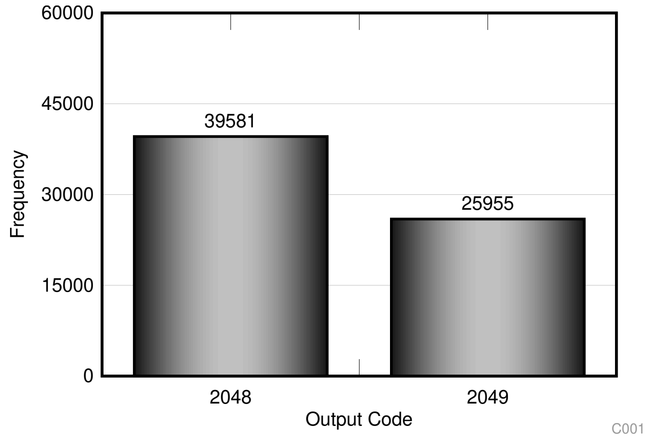


NOTE: S = start, Sr = repeated start, and P = stop.

Figure 1. I²C Timing Diagram

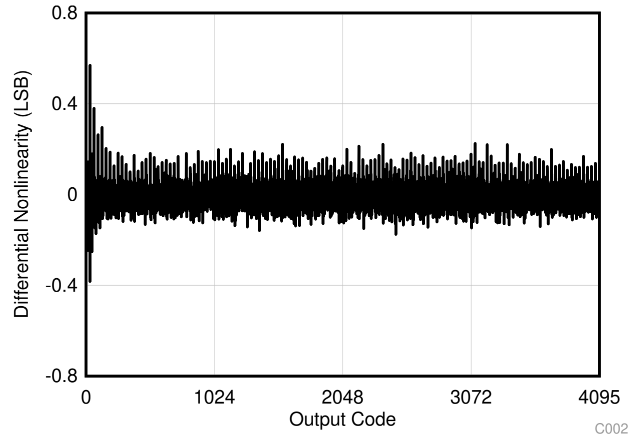
6.10 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and maximum throughput (unless otherwise noted)



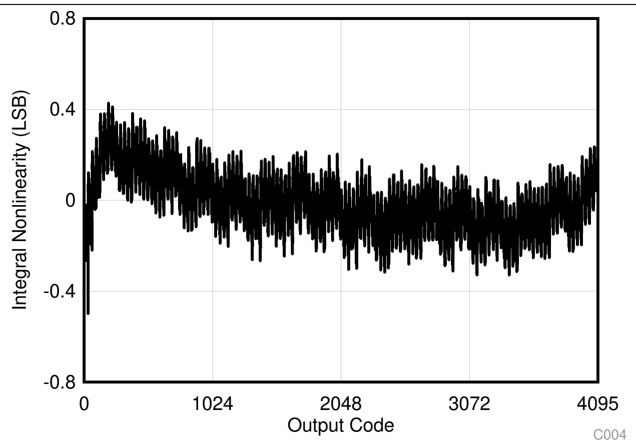
Standard deviation = 0.49 LSB

Figure 2. DC Input Histogram



Typical DNL = ±0.2 LSB

Figure 3. Typical DNL



Typical INL = ±0.5 LSB

Figure 4. Typical INL

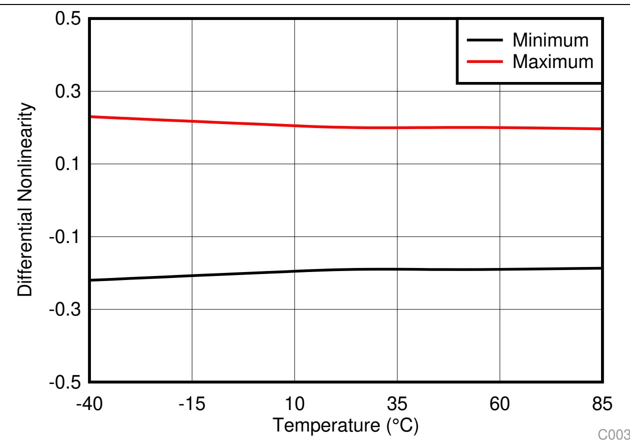


Figure 5. DNL vs Temperature

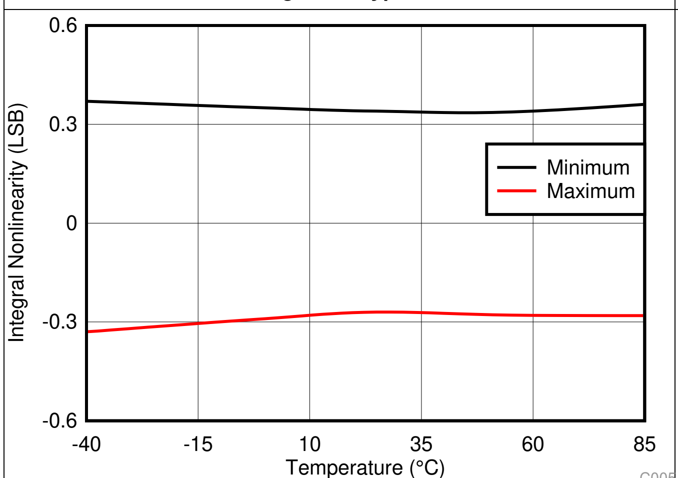


Figure 6. INL vs Temperature

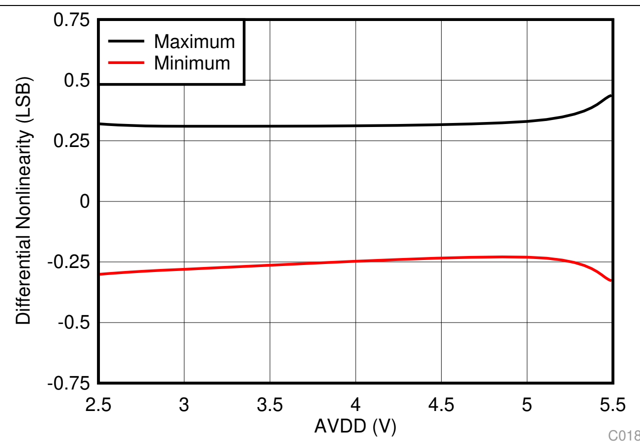


Figure 7. DNL vs AVDD

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and maximum throughput (unless otherwise noted)

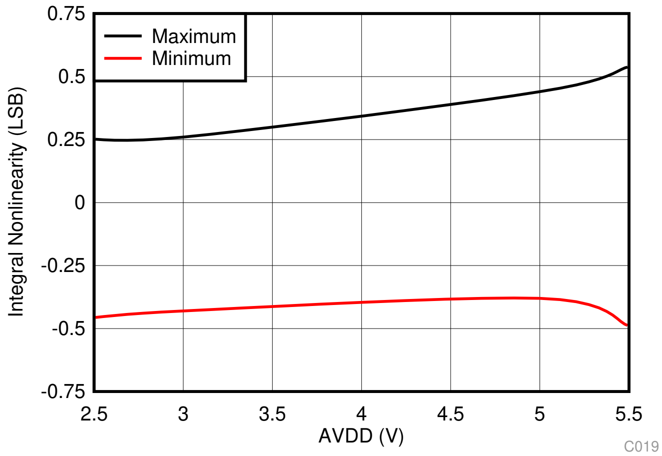


Figure 8. INL vs AVDD

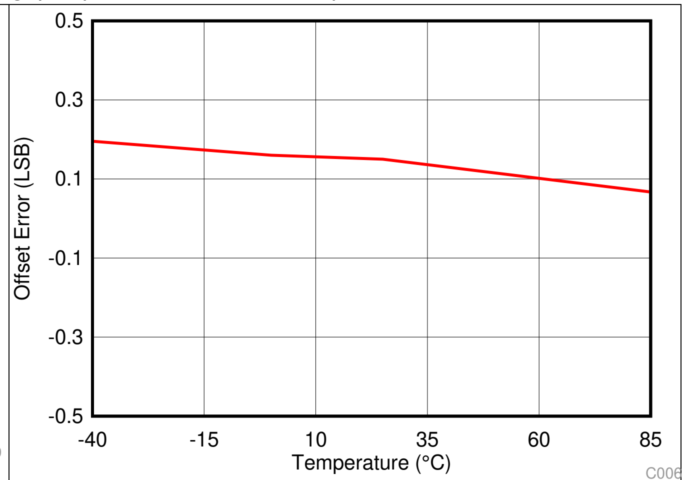


Figure 9. Offset Error vs Temperature

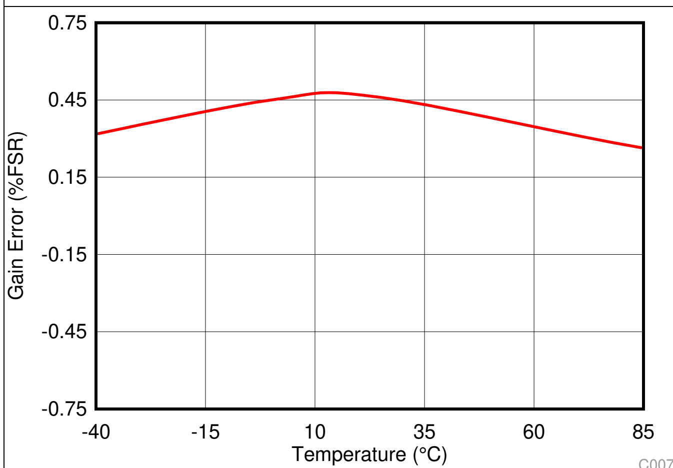


Figure 10. Gain Error vs Temperature

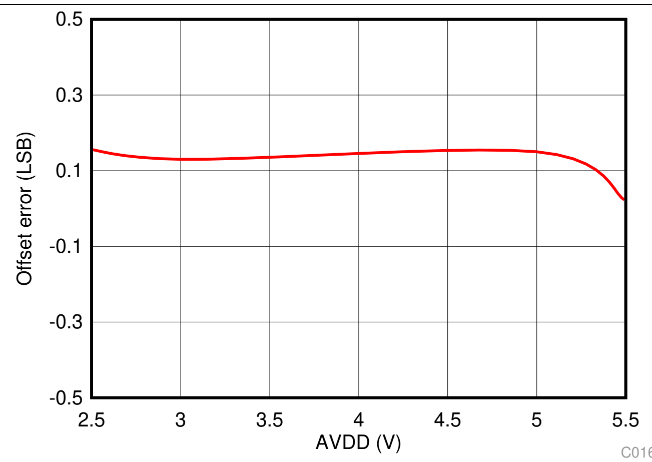


Figure 11. Offset Error vs AVDD

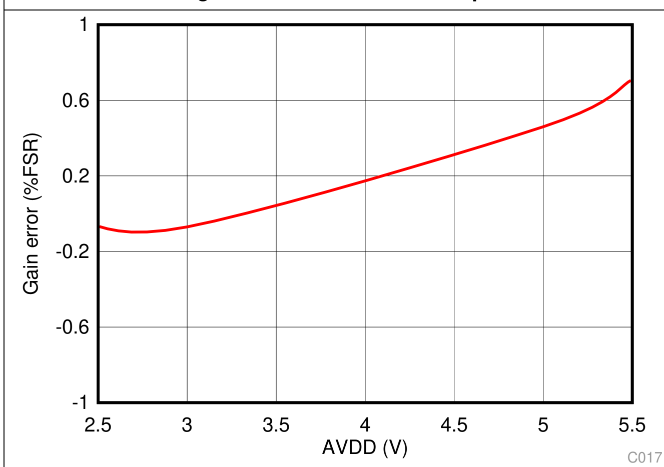
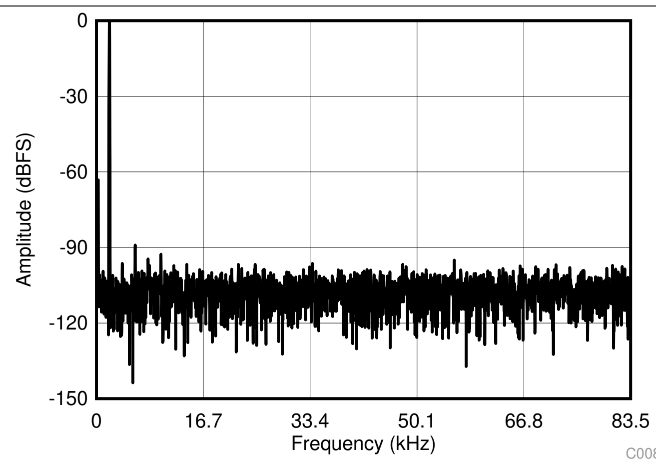


Figure 12. Gain Error vs AVDD



f_{IN} = 2 kHz, SNR = 73.2 dB, THD = 92.3 dB

Figure 13. Typical FFT

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and maximum throughput (unless otherwise noted)

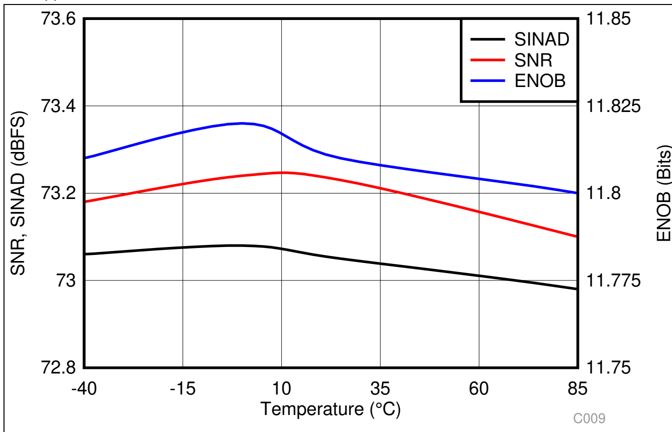


Figure 14. Noise Performance vs Temperature

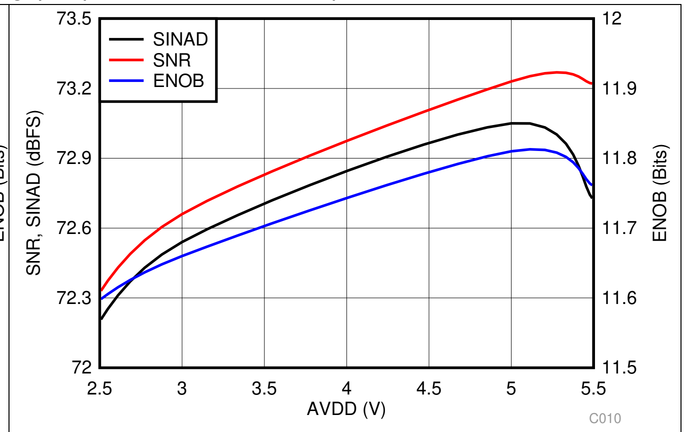


Figure 15. Noise Performance vs AVDD

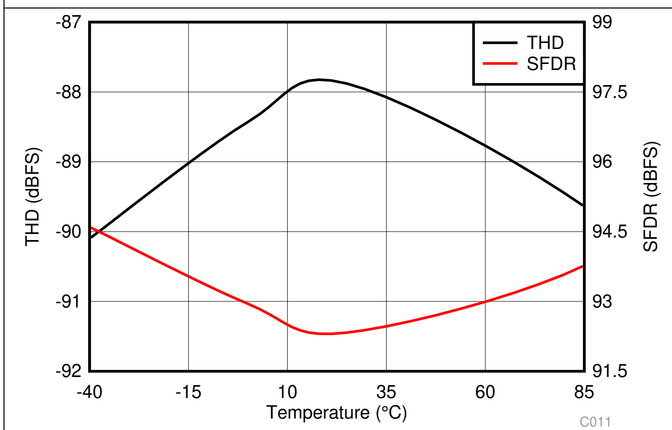


Figure 16. Distortion Performance vs Temperature

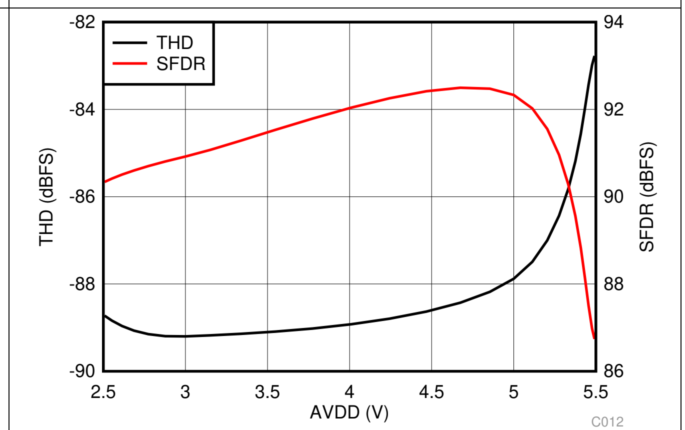


Figure 17. Distortion Performance vs AVDD

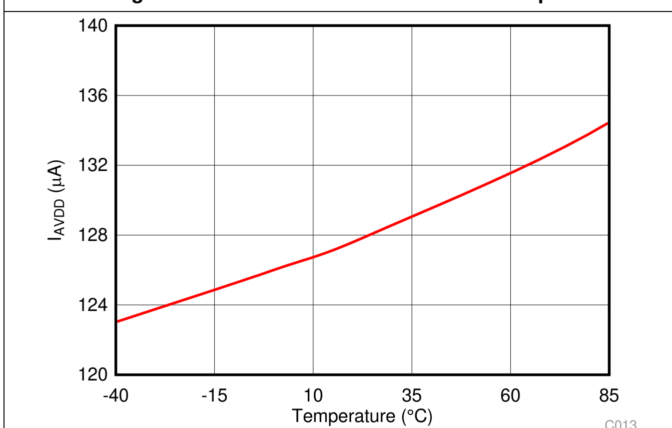


Figure 18. Analog Supply Current vs Temperature

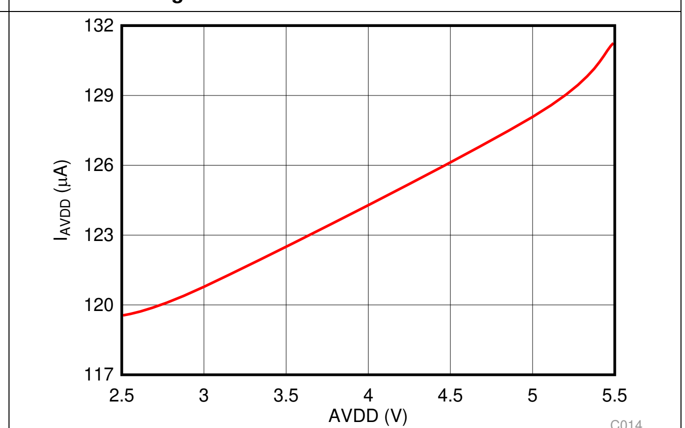


Figure 19. Analog Supply Current vs AVDD

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and maximum throughput (unless otherwise noted)

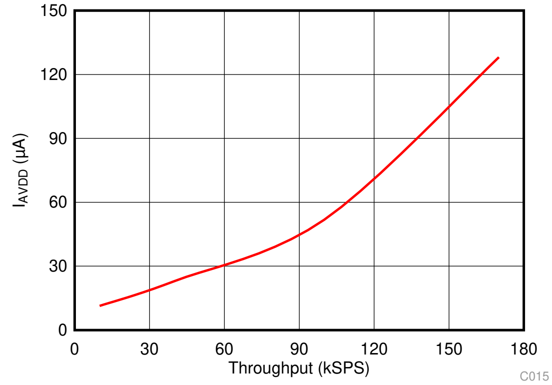


Figure 20. Analog Supply Current vs Throughput

7 Detailed Description

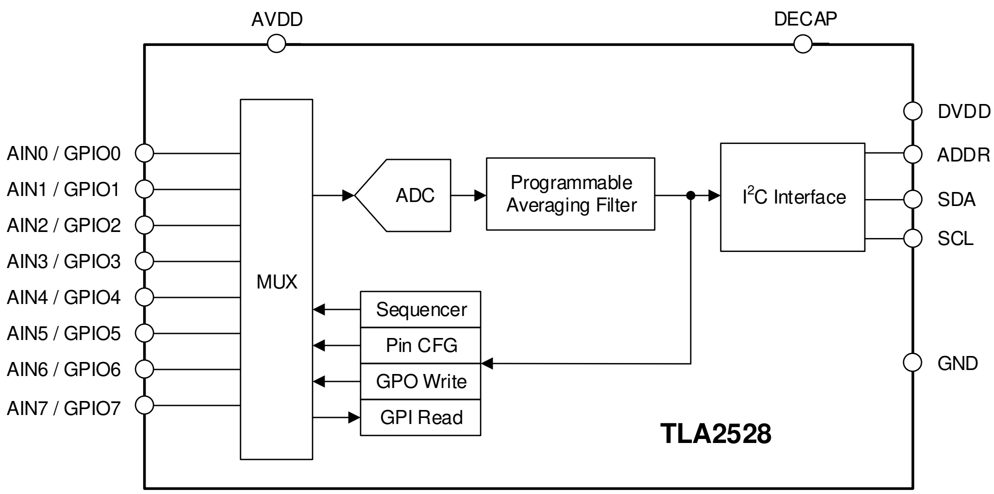
7.1 Overview

The TLA2528 is a small, eight-channel, multiplexed, 12-bit, analog-to-digital converter (ADC) with an I^2C-compatible serial interface. The eight channels of the TLA2528 can be individually configured as either analog inputs, digital inputs, or digital outputs. The device uses an internal oscillator for conversion. The analog input channel selection can be auto-sequenced to simplify the digital interface with the host.

The device features a programmable averaging filter that outputs a 16-bit result for enhanced resolution.

The I^2C serial interface supports standard-mode, fast-mode, fast-mode plus, and high-speed mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Multiplexer and ADC

The eight channels of the multiplexer can be independently configured as ADC inputs or general-purpose inputs/outputs (GPIOs). Figure 21 shows that each input pin has electrostatic discharge (ESD) protection diodes to AVDD and GND. On power-up or after device reset, all eight multiplexer channels are configured as analog inputs.

Figure 21 shows an equivalent circuit for pins configured as analog inputs. The ADC sampling switch is represented by an ideal switch (SW) in series with the resistor, R_{SW} (typically 150 Ω), and the sampling capacitor, C_{SH} (typically 12 pF).

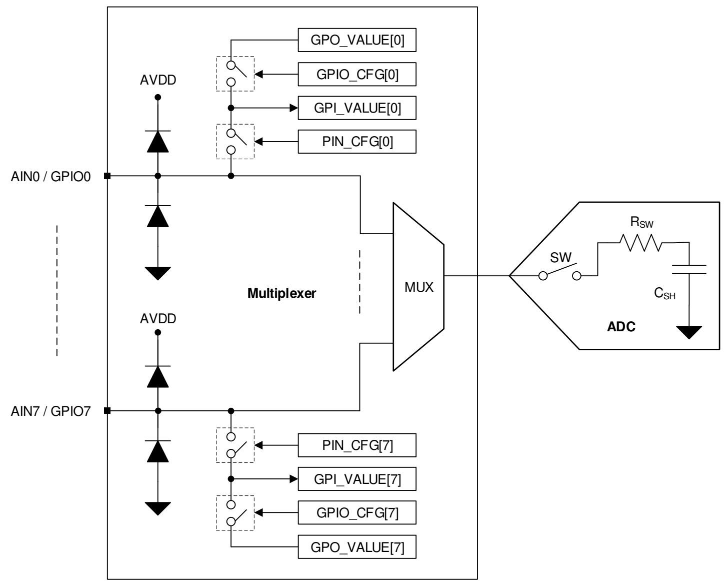


Figure 21. Analog Inputs, GPIOs, and ADC Connections

During acquisition, the SW switch is closed to allow the signal on the selected analog input channel to charge the internal sampling capacitor. During conversion, the SW switch is opened to disconnect the analog input channel from the sampling capacitor.

The multiplexer channels can be configured as GPIOs in the PIN_CFG register. The direction of a GPIO (either as an input or an output) can be set in the GPIO_CFG register. The logic level on the channels configured as digital I/O can be read from the GPI_VALUE register. The digital outputs can be accessed by writing to the GPO_VALUE register. The digital outputs can be configured as either open-drain or push-pull in the GPO_DRIVE_CFG register.

7.3.2 Reference

The device uses the analog supply voltage (AVDD) as a reference for the analog-to-digital conversion process. TI recommends connecting a 1-µF, low-equivalent series resistance (ESR) ceramic decoupling capacitor between the AVDD and GND pins.

7.3.3 ADC Transfer Function

The ADC output is in straight binary format. Equation 1 computes the ADC resolution:

$$1\ \text{LSB} = V_{REF} / 2^N$$

where:

- V_{REF} = AVDD
- N = 12 (1)

Figure 22 and Table 1 detail the transfer characteristics for the device.

Feature Description (continued)

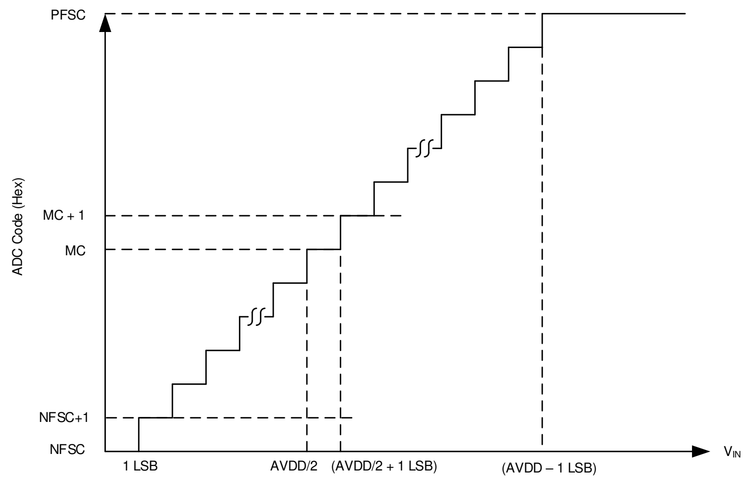


Figure 22. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

INPUT VOLTAGE	CODE	DESCRIPTION	IDEAL OUTPUT CODE
≤1 LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	NFSC + 1	—	001
(AVDD / 2) to (AVDD / 2) + 1 LSB	MC	Mid code	800
(AVDD / 2) + 1 LSB to (AVDD / 2) + 2 LSB	MC + 1	—	801
≥ AVDD – 1 LSB	PFSC	Positive full-scale code	FFF

7.3.4 ADC Offset Calibration

The variation in ADC offset error resulting from changes in temperature or AVDD can be calibrated by setting the CAL bit in the GENERAL_CFG register. The CAL bit is reset to 0 after calibration. The host can poll the CAL bit to check the ADC offset calibration completion status.

7.3.5 I^2C Address Selector

The I^2C address for the device is determined by connecting external resistors on the ADDR pin. The device address is determined at power-up based on the resistor values. The device retains this address until the next power-up event, until the next device reset, or until the device receives a command to program its own address. Figure 23 shows a connection diagram for the ADDR pin and Table 2 lists the resistor values for selecting different addresses of the device.

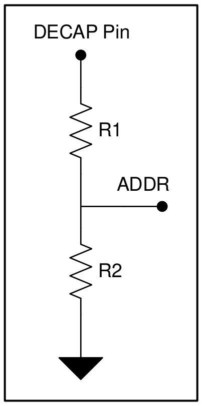


Figure 23. External Resistor Connection Diagram for the ADDR Pin

Table 2. I²C Address Selection

RESISTORS		ADDRESS
R1 (1)	R2 (1)	
0 Ω	DNP (2)	001 0111b (17h)
11 kΩ	DNP (2)	001 0110b (16h)
33 kΩ	DNP (2)	001 0101b (15h)
100 kΩ	DNP (2)	001 0100b (14h)
DNP (2)	DNP (2)	001 0000b (10h)
DNP (2)	11 kΩ	001 0001b (11h)
DNP (2)	33 kΩ	001 0010b (12h)
DNP (2)	100 kΩ	001 0011b (13h)

(1) Tolerance for R1, R2 ≤ ±5%.
(2) DNP = Do not populate.

7.3.6 Programmable Averaging Filter

The ADS7138 features a built-in oversampling (OSR) function that can be used to average several samples. The averaging filter can be enabled by programming the OSR[2:0] bits in the OSR_CFG register. The averaging filter configuration is common to all analog input channels. Figure 24 shows that the averaging filter module output is 16 bits long. In the manual conversion mode and auto-sequence mode, only the first conversion for the selected analog input channel must be initiated by the host; see the *Manual Mode* and *Auto-Sequence Mode* sections. As shown in Figure 24, any remaining conversions for the selected averaging factor are generated internally. The time required to complete the averaging operation is determined by the sampling speed and number of samples to be averaged. As shown in Figure 24, the 16-bit result can be read out after the averaging operation completes.

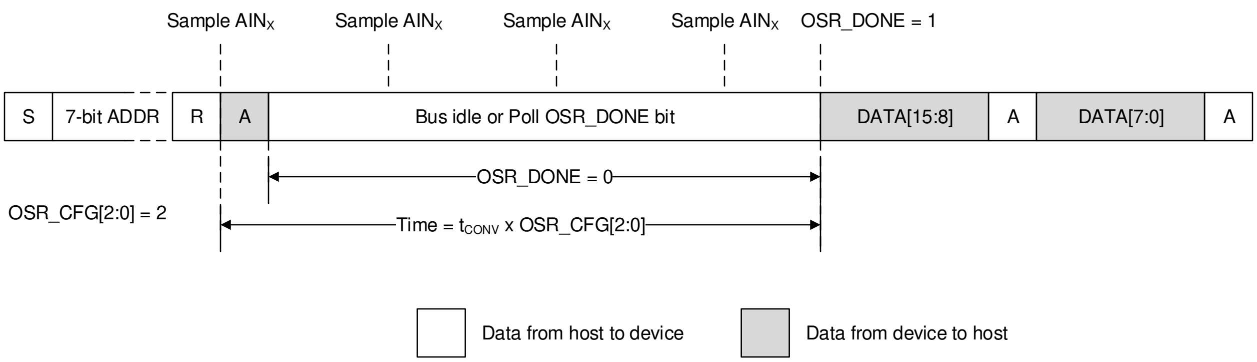


Figure 24. Averaging Example

In Figure 24, SCL is stretched by the device after the start of conversions until the averaging operation is complete.

If SCL stretching is not required during averaging, enable the statistics registers by setting STATS_EN to 1b and initiate conversions by writing 1b to the CNVST bit. The OSR_DONE bit in the SYSTEM_STATUS register can be polled to check the averaging completion status. When using the CNVST bit to initiate conversion, the result can be read in the RECENT_CHx_LSB and RECENT_CHx_MSB registers.

Equation 2 provides the LSB value of the 16-bit average result.

$$1\ LSB = \frac{AVDD}{2^{16}} \quad (2)$$

7.3.7 General-Purpose I/Os (GPIOs)

The eight channels of the TLA2528 can be independently configured as analog inputs, digital inputs, or digital outputs. Table 3 describes how the PIN_CFG and GPIO_CFG registers can be used to configure the channels.

Table 3. Configuring Channels as Analog Inputs or GPIOs

PIN_CFG[7:0]	GPIO_CFG[7:0]	GPO_DRIVE_CFG[7:0]	CHANNEL CONFIGURATION
0	x	x	Analog input (default)
1	0	x	Digital input
1	1	0	Digital output; open-drain driver
1	1	1	Digital output; push-pull driver

The digital outputs can be configured to logic 1 or 0 by writing to the GPO_VALUE register. Reading the GPI_VALUE register returns the logic level for all channels configured as digital inputs.

7.3.8 Oscillator and Timing Control

The device uses an internal oscillator for conversions. When using the averaging module, the host initiates the first conversion and all subsequent conversions are generated internally by the device. However, in the autonomous mode of operation, the start of the conversion signal is generated by the device. Table 4 shows that when the device generates the start of the conversion, the sampling rate is controlled by the OSC_SEL and CLK_DIV[3:0] register fields.

Table 4. Configuring Sampling Rate for Internal Conversion Start Control

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	SAMPLING FREQUENCY, f_{CYCLE} (kSPS)	CYCLE TIME, t_{CYCLE} (µs)	SAMPLING FREQUENCY, f_{CYCLE} (kSPS)	CYCLE TIME, t_{CYCLE} (µs)
0000b	1000	1	31.25	32
0001b	666.7	1.5	20.83	48
0010b	500	2	15.63	64
0011b	333.3	3	10.42	96
0100b	250	4	7.81	128
0101b	166.7	6	5.21	192
0110b	125	8	3.91	256
0111b	83	12	2.60	384
1000b	62.5	16	1.95	512
1001b	41.7	24	1.3	768
1010b	31.3	32	0.98	1024
1011b	20.8	48	0.65	1536
1100b	15.6	64	0.49	2048
1101b	10.4	96	0.33	3072
1110b	7.8	128	0.24	4096
1111b	5.2	192	0.16	6144

The conversion time of the device (see t_{CONV} in the *Switching Characteristics* table) is independent of the OSC_SEL and CLK_DIV[3:0] configuration.

7.3.9 Output Data Format

Figure 25 illustrates various I^2C frames for reading data.

- Read the ADC conversion result: Two 8-bit I^2C packets are required (frame A).
- Read the averaged conversion result: Two 8-bit I^2C packets are required (frame B).
- Read data with the channel ID appended: The 4-bit channel ID can be appended to the 12-bit ADC result by configuring the APPEND_STATUS field in the GENERAL_CFG register. When the channel ID is appended to the 12-bit ADC data, two I^2C packets are required (frame C). If the channel ID is appended to the 16-bit average result, three I^2C frames are required (frame D).

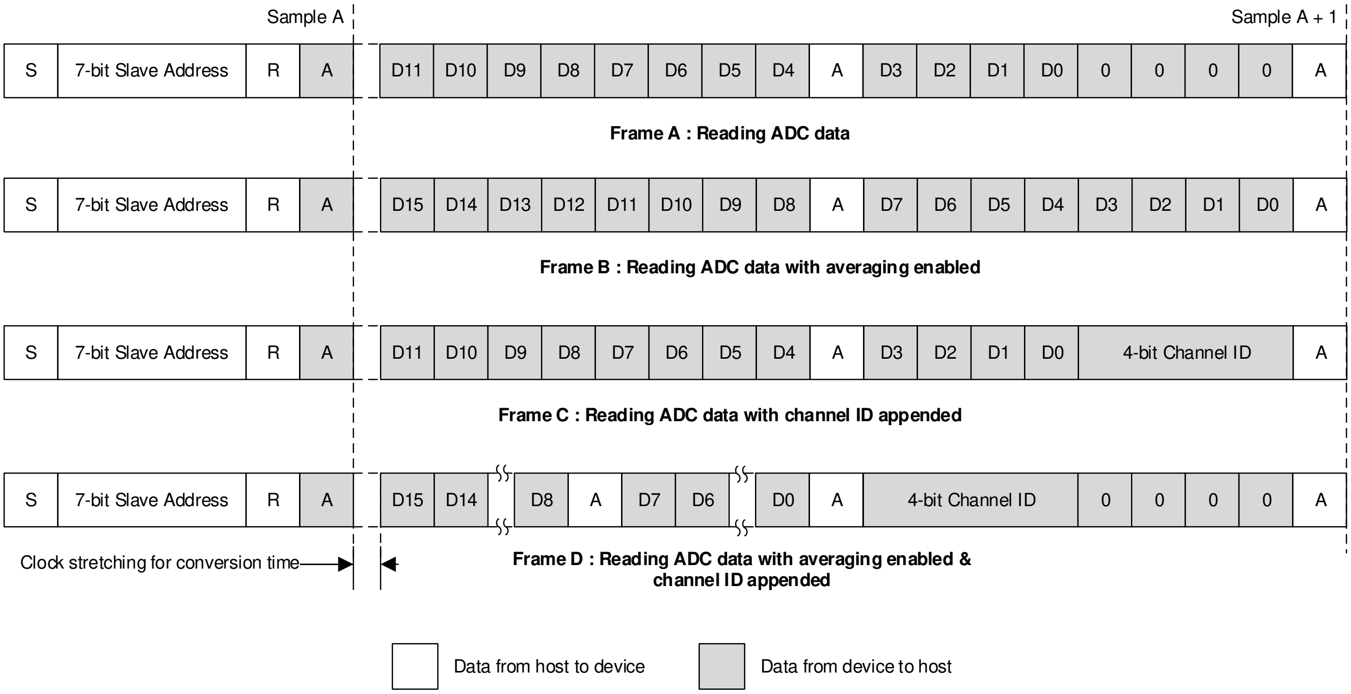


Figure 25. Data Frames for Reading Data

7.3.10 I²C Protocol Features

7.3.10.1 General Call

On receiving a general call (00h), the device provides an acknowledge (ACK).

7.3.10.2 General Call With Software Reset

On receiving a general call (00h) followed by a software reset (06h), the device resets itself.

7.3.10.3 General Call With a Software Write to the Programmable Part of the Slave Address

On receiving a general call (00h) followed by 04h, the device reevaluates its own I²C address configured by the ADDR pin. During this operation, the device does not respond to other I²C commands except the general-call command.

7.3.10.4 Configuring the Device for High-Speed I²C Mode

The device can be configured in high-speed I²C mode by providing an I²C frame with one of these codes: 0x09, 0x0B, 0x0D, or 0x0F.

After receiving one of these codes, the device sets the I2C_HIGH_SPEED bit in the SYSTEM_STATUS register and remains in high-speed I²C mode until a STOP condition is received in an I²C frame.

7.4 Device Functional Modes

Table 5 lists the functional modes supported by the TLA2528.

Table 5. Functional Modes

FUNCTIONAL MODE	CONVERSION CONTROL	MUX CONTROL	SEQ_MODE[1:0]
Manual	9th falling edge of SCL (ACK)	Register write to MANUAL_CHID	00b
Auto-sequence	9th falling edge of SCL (ACK)	Channel sequencer	01b

The device powers up in manual mode (see the *Manual Mode* section) and can be configured into any mode listed in Table 5 by writing the configuration registers for the desired mode.

7.4.1 Device Power-Up and Reset

On power-up, the device calculates the address from the resistors connected on the ADDR pin and the BOR bit is set, thus indicating a power-cycle or reset event.

The device can be reset by an I^2C general call (00h) followed by a software reset (06h), by setting the RST bit, or by recycling the power on the AVDD pin.

7.4.2 Manual Mode

Manual mode allows the external host processor to directly select the analog input channel. Figure 26 lists the steps for operating the device in manual mode.

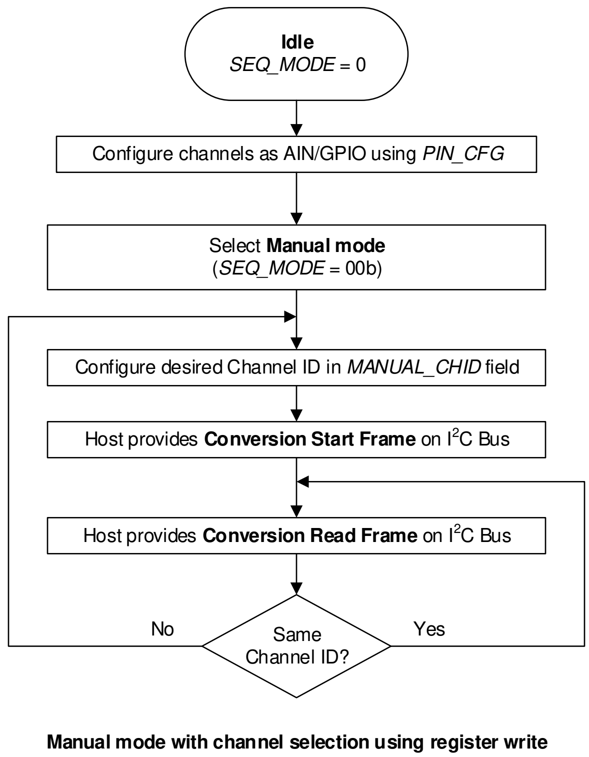


Figure 26. Device Operation in Manual Mode

Provide an I^2C start or restart frame to initiate a conversion, as shown in the conversion start frame of Figure 27, after configuring the device registers. ADC data can be read in subsequent I^2C frames. The number of I^2C frames required to read conversion data depends on the output data frame size; see the *Output Data Format* section for more details. A new conversion is initiated on the ninth falling edge of SCL (ACK bit) when the last byte of output data is read.

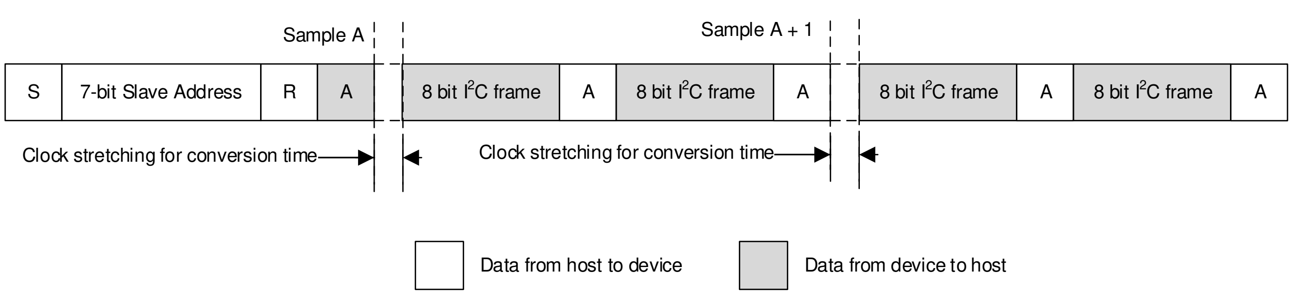


Figure 27. Starting a Conversion and Reading Data in Manual Mode

7.4.3 Auto-Sequence Mode

In auto-sequence mode, the internal channel sequencer switches the multiplexer to the next analog input channel after every conversion. The desired analog input channels can be configured for sequencing in the AUTO_SEQ_CHSEL register. To enable the channel sequencer, set SEQ_START to 1b. After every conversion, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ_START to 0b. Figure 28 lists the conversion start and read frames for auto-sequence mode.

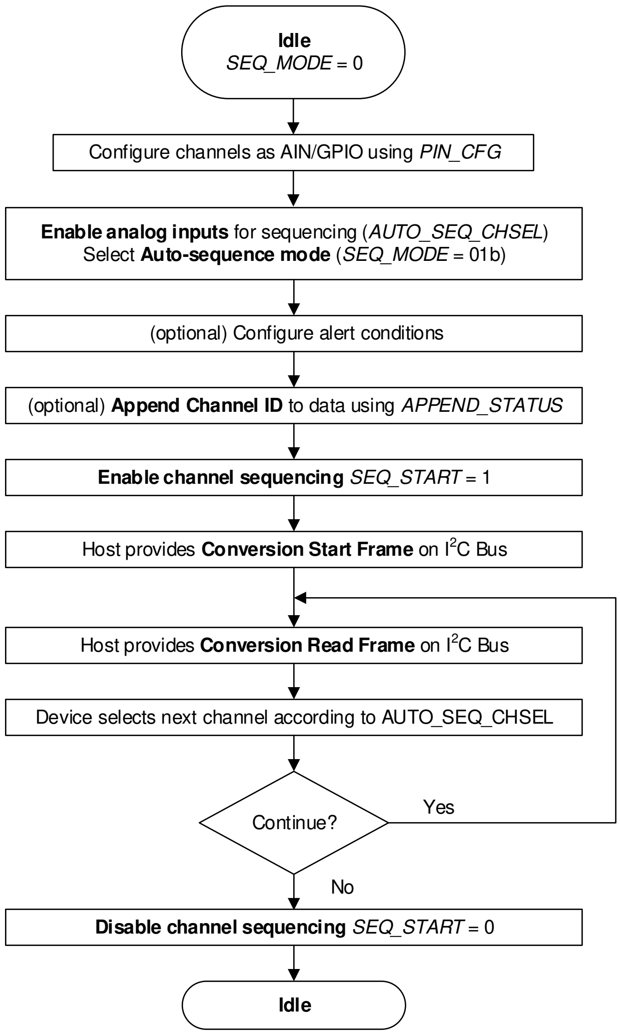


Figure 28. Device Operation in Auto-Sequence Mode

7.5 Programming

Table 6 provides the acronyms for different conditions in an I²C frame. Table 7 lists the various command opcodes.

Table 6. I²C Frame Acronyms

SYMBOL	DESCRIPTION
S	Start condition for the I²C frame
Sr	Restart condition for the I²C frame
P	Stop condition for the I²C frame
A	ACK (low)
N	NACK (high)
R	Read bit (high)
W	Write bit (low)

Table 7. Opcodes for Commands

OPCODE	COMMAND DESCRIPTION
0001 0000b	Single register read
0000 1000b	Single register write
0001 1000b	Set bit
0010 0000b	Clear bit
0011 0000b	Reading a continuous block of registers
0010 1000b	Writing a continuous block of registers

7.5.1 Reading Registers

The I²C master can either read a single register or a continuous block registers from the device, as described in the *Single Register Read* and *Reading a Continuous Block of Registers* sections.

7.5.1.1 Single Register Read

To read a single register from the device, the I²C master must provide an I²C command with three frames to set the register address for reading data. Table 7 lists the opcodes for different commands. After this command is provided, the I²C master must provide another I²C frame (as shown in Figure 29) containing the device address and the read bit. After this frame, the device provides the register data. The device provides the same register data even if the host provides more clocks. To end the register read command, the master must provide a STOP or a RESTART condition in the I²C frame.

S	7-bit Slave Address	W	A	0001 0000b	A	Register Address	A	P/Sr	S	7-bit Slave Address	R	A	Register Data	A	P/Sr

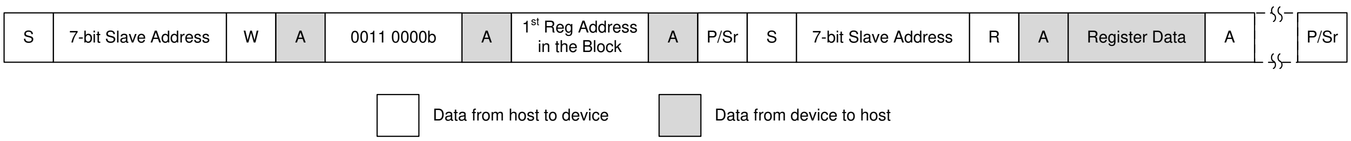
Data from host to device   Data from device to host

NOTE: S = start, Sr = repeated start, and P = stop.

Figure 29. Reading Register Data

7.5.1.2 Reading a Continuous Block of Registers

To read a continuous block of registers, the I^{2}C master must provide an I^{2}C command to set the register address. The register address is the address of the first register in the block that must be read. After this command is provided, the I^{2}C master must provide another I^{2}C frame, as shown in Figure 30, containing the device address and the read bit. After this frame, the device provides the register data. The device provides data for the next register when more clocks are provided. When data are read from addresses that do not exist in the register map of the device, the device returns zeros. If the device does not have any further registers to provide data on, the device provide zeros. To end the register read command, the master must provide a STOP or a RESTART condition in the I^{2}C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

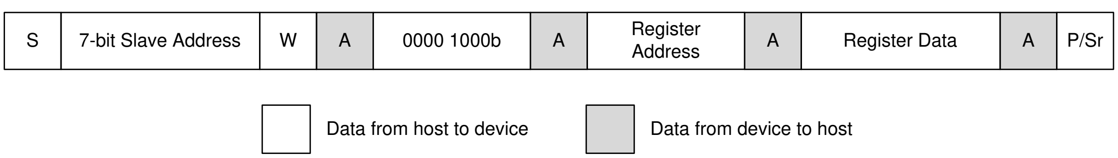
Figure 30. Reading a Continuous Block of Registers

7.5.2 Writing Registers

The I^{2}C master can either write a single register or a continuous block of registers to the device, set a few bits in a register, or clear a few bits in a register.

7.5.2.1 Single Register Write

To write a single register from the device, as shown in Figure 31, the I^{2}C master must provide an I^{2}C command with four frames. The register address is the address of the register that must be written and the register data is the value that must be written. Table 7 lists the opcodes for different commands. To end the register write command, the master must provide a STOP or a RESTART condition in the I^{2}C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

Figure 31. Writing a Single Register

7.5.2.2 Set Bit

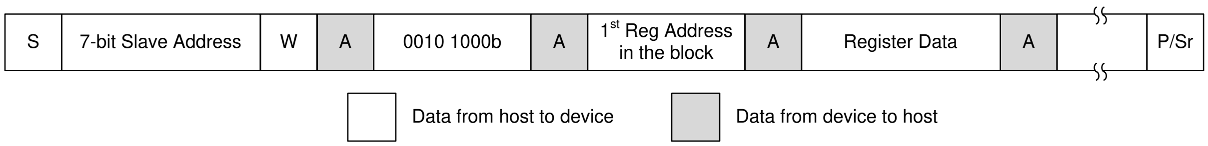
The I^{2}C master must provide an I^{2}C command with four frames, as shown in Figure 31, to set bits in a register without changing the other bits. The register address is the address of the register that the bits must set and the register data is the value representing the bits that must be set. Bits with a value of 1 in the register data are set and bits with a value of 0 in the register data are not changed. Table 7 lists the opcodes for different commands. To end this command, the master must provide a STOP or RESTART condition in the I^{2}C frame.

7.5.2.3 Clear Bit

The I^{2}C master must provide an I^{2}C command with four frames, as shown in Figure 31, to clear bits in a register without changing the other bits. The register address is the address of the register that the bits must clear and the register data is the value representing the bits that must be cleared. Bits with a value of 1 in the register data are cleared and bits with a value of 0 in the register data are not changed. Table 7 lists the opcodes for different commands. To end this command, the master must provide a STOP or a RESTART condition in the I^{2}C frame.

7.5.2.4 Writing a Continuous Block of Registers

The I^{2}C master must provide an I^{2}C command, as shown in Figure 32, to write a continuous block of registers. The register address is the address of the first register in the block that must be written. The I^{2}C master must provide data for registers in subsequent I^{2}C frames in an ascending order of register addresses. Writing data to addresses that do not exist in the register map of the device have no effect. Table 7 lists the opcodes for different commands. If the data provided by the I^{2}C master exceeds the address space of the device, the device ignores the data beyond the address space. To end the register write command, the master must provide a STOP or a RESTART condition in the I^{2}C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

Figure 32. Writing a Continuous Block of Registers

7.6 TLA2528 Registers

Table 8 lists the TLA2528 registers. All register offset addresses not listed in Table 8 should be considered as reserved locations and the register contents should not be modified.

Table 8. TLA2528 Registers

Address	Acronym	Register Name	Section
0x0	SYSTEM_STATUS		SYSTEM_STATUS Register (Address = 0x0) [reset = 0x80]
0x1	GENERAL_CFG		GENERAL_CFG Register (Address = 0x1) [reset = 0x0]
0x2	DATA_CFG		DATA_CFG Register (Address = 0x2) [reset = 0x0]
0x3	OSR_CFG		OSR_CFG Register (Address = 0x3) [reset = 0x0]
0x4	OPMODE_CFG		OPMODE_CFG Register (Address = 0x4) [reset = 0x0]
0x5	PIN_CFG		PIN_CFG Register (Address = 0x5) [reset = 0x0]
0x7	GPIO_CFG		GPIO_CFG Register (Address = 0x7) [reset = 0x0]
0x9	GPO_DRIVE_CFG		GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]
0xB	GPO_VALUE		GPO_VALUE Register (Address = 0xB) [reset = 0x0]
0xD	GPI_VALUE		GPI_VALUE Register (Address = 0xD) [reset = 0x0]
0x10	SEQUENCE_CFG		SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]
0x11	CHANNEL_SEL		CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]
0x12	AUTO_SEQ_CH_SEL		AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]

Complex bit access types are encoded to fit into small table cells. Table 9 shows the codes that are used for access types in this section.

Table 9. TLA2528 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

7.6.1 SYSTEM_STATUS Register (Address = 0x0) [reset = 0x80]

SYSTEM_STATUS is shown in Figure 33 and described in Table 10.

Return to the Summary Table.

Figure 33. SYSTEM_STATUS Register

7	6	5	4	3	2	1	0
RSVD	SEQ_STATUS	I^{2}C_SPEED	RESERVED	OSR_DONE	CRC_ERR_FUSE	RESERVED	BOR
R-1b	R-0b	R-0b	R-0b	R/W-0b	R-0b	R-0b	R/W-0b

Table 10. SYSTEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	1b	This bit must read 1b.
6	SEQ_STATUS	R	0b	Sequencer Status 0b = Sequence stopped 1b = Sequence in progress
5	I^{2}C_SPEED	R	0b	I^{2}C high-speed status 0b = Device is not in high speed mode 1b = Device is in high speed mode
4	RESERVED	R	0b	Reserved. Reads return 0b.
3	OSR_DONE	R/W	0b	OSR status. Clear this bit by writing 1b to this bit. 0b = OSR in progress; data not ready. 1b = OSR complete; data ready.
2	CRC_ERR_FUSE	R	0b	Device fuse CRC check status. To re-evaluate this bit, software reset the device or power cycle AVDD. 0b = Configuration is good. 1b = Device configuration not loaded correctly.
1	RESERVED	R	0b	Reserved. Reads return 0b.
0	BOR	R/W	0b	Brown out reset indicator. This bit is set if brown out condition occurs or device is power cycled. Write 1 to this bit to clear the flag. 0b = No brown out from last time this bit was cleared. 1b = Brown out condition detected or device power cycled.

7.6.2 GENERAL_CFG Register (Address = 0x1) [reset = 0x0]

GENERAL_CFG is shown in Figure 34 and described in Table 11.

Return to the Summary Table.

Figure 34. GENERAL_CFG Register

7	6	5	4	3	2	1	0
RESERVED				CNVST	CH_RST	CAL	RST
R-0b				W-0b	R/W-0b	R/W-0b	W-0b

Table 11. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved. Reads return 0b.
3	CNVST	W	0b	Intiate start of conversion. Readback of this bit will return 0. 0b = Normal operation. 1b = Initiate start of conversion.
2	CH_RST	R/W	0b	Force all channels to be analog inputs. 0b = Normal operation. 1b = All channels will be set as analog inputs irrespective of configuration in other registers.
1	CAL	R/W	0b	Calibrate ADC offset. 0b = Normal operation. 1b = ADC offset will be calibrated. After calibration is complete, this bit will be set to 0.

Table 11. GENERAL_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RST	W	0b	Software reset all registers to default values. 0b = Normal operation. 1b = Device will be reset. After reset is complete, this bit will be set to 0.

7.6.3 DATA_CFG Register (Address = 0x2) [reset = 0x0]

DATA_CFG is shown in Figure 35 and described in Table 12.

Return to the Summary Table.

Figure 35. DATA_CFG Register

7	6	5	4	3	2	1	0
FIX_PAT	RESERVED	APPEND_STATUS[1:0]		RESERVED			
R/W-0b	R-0b	R/W-0b		R-0b			

Table 12. DATA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIX_PAT	R/W	0b	Device outputs fixed data bits. Helpful for debugging device communication. 0b = Normal operation. 1b = Device outputs a fixed code 0xA5A repeatitively when reading ADC data.
6	RESERVED	R	0b	Reserved. Reads return 0b.
5-4	APPEND_STATUS[1:0]	R/W	0b	Append 4-bit channel ID to output data. 0b = Channel ID is not appended to ADC data. 1b = Channel ID is appended to ADC data.
3-0	RESERVED	R	0b	Reserved. Reads return 0b.

7.6.4 OSR_CFG Register (Address = 0x3) [reset = 0x0]

OSR_CFG is shown in Figure 36 and described in Table 13.

Return to the Summary Table.

Figure 36. OSR_CFG Register

7	6	5	4	3	2	1	0
RESERVED					OSR[2:0]		
R-0b					R/W-0b		

Table 13. OSR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0b.
2-0	OSR[2:0]	R/W	0b	Selects the oversampling ratio for ADC conversion result. 0b = OSR = 0. 1b = OSR = 2. 10b = OSR = 4. 11b = OSR = 8. 100b = OSR = 16. 101b = OSR = 32. 110b = OSR = 64. 111b = OSR = 128.

7.6.5 OPMODE_CFG Register (Address = 0x4) [reset = 0x0]

OPMODE_CFG is shown in Figure 37 and described in Table 14.

Return to the Summary Table.

Figure 37. OPMODE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			OSC_SEL	CLK_DIV[3:0]			
R-0b			R/W-0b	R/W-0b			

Table 14. OPMODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0b.
4	OSC_SEL	R/W	0b	Selects the oscillator for internal timing generation. 0b = High speed oscillator. 1b = Low power oscillator.
3-0	CLK_DIV[3:0]	R/W	0b	Sampling speed control. Refer to section on Oscillator and Timing Control for details.

7.6.6 PIN_CFG Register (Address = 0x5) [reset = 0x0]

PIN_CFG is shown in Figure 38 and described in Table 15.

Return to the Summary Table.

Figure 38. PIN_CFG Register

7	6	5	4	3	2	1	0
PIN_CFG[7:0]							
R/W-0b							

Table 15. PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PIN_CFG[7:0]	R/W	0b	Configure device channels CH7 through CH0 as analog input or GPIO. 0b = Channel is configured as analog input. 1b = Channel is configured as GPIO.

7.6.7 GPIO_CFG Register (Address = 0x7) [reset = 0x0]

GPIO_CFG is shown in Figure 39 and described in Table 16.

Return to the Summary Table.

Figure 39. GPIO_CFG Register

7	6	5	4	3	2	1	0
GPIO_CFG[7:0]							
R/W-0b							

Table 16. GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_CFG[7:0]	R/W	0b	Configure GPIO7 through GPIO0 as either digital input or digital output. 0b = GPIO is digital input. 1b = GPIO is digital output.

7.6.8 GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]

GPO_DRIVE_CFG is shown in Figure 40 and described in Table 17.

Return to the Summary Table.

Figure 40. GPO_DRIVE_CFG Register

7	6	5	4	3	2	1	0
GPO_DRIVE_CFG[7:0]							
R/W-0b							

Table 17. GPO_DRIVE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_DRIVE_CFG[7:0]	R/W	0b	Configure digital outputs GPO7 through GPO0 as open-drain or push-pull output. 0b = Digital output is open-drain. Connect external pullup. 1b = Digital output is push-pull.

7.6.9 GPO_VALUE Register (Address = 0xB) [reset = 0x0]

GPO_VALUE is shown in Figure 41 and described in Table 18.

Return to the Summary Table.

Figure 41. GPO_VALUE Register

7	6	5	4	3	2	1	0
GPO_VALUE[7:0]							
R/W-0b							

Table 18. GPO_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE[7:0]	R/W	0b	Logic level to be set on digital outputs GPO[7:0]. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

7.6.10 GPI_VALUE Register (Address = 0xD) [reset = 0x0]

GPI_VALUE is shown in Figure 42 and described in Table 19.

Return to the Summary Table.

Figure 42. GPI_VALUE Register

7	6	5	4	3	2	1	0
GPI_VALUE[7:0]							
R-0b							

Table 19. GPI_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPI_VALUE[7:0]	R	0b	Readback the logic level on digital input. 0b = Digital input is at logic 0. 1b = Digital input is at logic 1.

7.6.11 SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]

SEQUENCE_CFG is shown in Figure 43 and described in Table 20.

Return to the Summary Table.

Figure 43. SEQUENCE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			SEQ_START	RESERVED		SEQ_MODE[1:0]	
R-0b			R/W-0b	R-0b		R/W-0b	

Table 20. SEQUENCE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0b.
4	SEQ_START	R/W	0b	Sequence start control when using auto sequence mode. 0b = Stop auto sequencing. 1b = Start auto sequencing from first enabled analog input channel starting from channel ID = 0 (ascending order).
3-2	RESERVED	R	0b	Reserved. Reads return 0b.
1-0	SEQ_MODE[1:0]	R/W	0b	Selects the mode of scanning analog input channels. 0b = Manual sequence mode. 1b = Auto sequence mode. 10b = Reserved. 11b = Reserved.

7.6.12 CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]

CHANNEL_SEL is shown in Figure 44 and described in Table 21.

Return to the Summary Table.

Figure 44. CHANNEL_SEL Register

7	6	5	4	3	2	1	0
RESERVED				MANUAL_CHID[3:0]			
R-0b				R/W-0b			

Table 21. CHANNEL_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved. Reads return 0b.
3-0	MANUAL_CHID[3:0]	R/W	0b	In manual mode, this field contains the 4-bit channel ID of the analog input channel for next ADC conversion. For valid ADC data, the channel ID must not be configured as GPIO. 0b = CH0 1b = CH1 10b = CH2 11b = CH3 100b = CH4 101b = CH5 110b = CH6 111b = CH7 1000b = Reserved.

7.6.13 AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]

AUTO_SEQ_CH_SEL is shown in Figure 45 and described in Table 22.

Return to the Summary Table.

Figure 45. AUTO_SEQ_CH_SEL Register

7	6	5	4	3	2	1	0
AUTO_SEQ_CH_SEL[7:0]							
R/W-0b							

Table 22. AUTO_SEQ_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_SEQ_CH_SEL[7:0]	R/W	0b	Enable analog input channels AIN7 through AIN0 in auto sequencing mode. 0b = Analog input channel is not enabled in scanning sequence. 1b = Analog input channel is enabled in scanning sequence.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Applications

8.2.1 Mixed-Channel Configuration

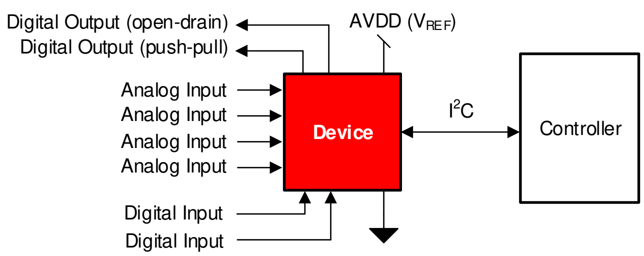


Figure 46. DAQ Circuit: Single-Supply DAQ

8.2.1.1 Design Requirements

The goal of this application is to configure some channels of the TLA2528 as digital inputs, open-drain digital outputs, and push-pull digital outputs.

8.2.1.2 Detailed Design Procedure

The TLA2528 can support GPIO functionality at each input pin. Any analog input pin can be independently configured as a digital input, a digital open-drain output, or a digital push-pull output though the PIN_CFG and GPIO_CFG registers; see Table 3.

8.2.1.2.1 Digital Input

The digital input functionality can be used to monitor a signal within the system. Figure 47 illustrates that the state of the digital input can be read from the GPI_VALUE register.

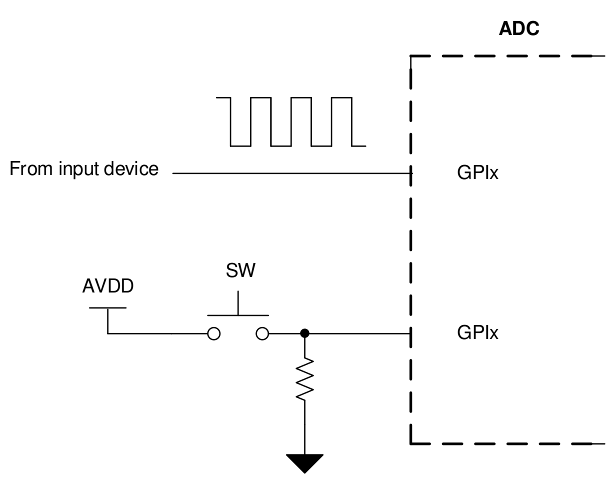


Figure 47. Digital Input

Typical Applications (continued)

8.2.1.2.2 Digital Open-Drain Output

The channels of the TLA2528 can be configured as digital open-drain outputs supporting an output voltage up to 5.5 V. An open-drain output, as shown in Figure 48, consists of an internal FET (Q) connected to ground. The output is idle when not driven by the device, which means Q is off and the pull-up resistor, R_{PULL_UP}, connects the GPOx node to the desired output voltage. The output voltage can range anywhere up to 5.5 V, depending on the external voltage that the GPIOx is pulled up to. When the device is driving the output, Q turns on, thus connecting the pull-up resistor to ground and bringing the node voltage at GPOx low.

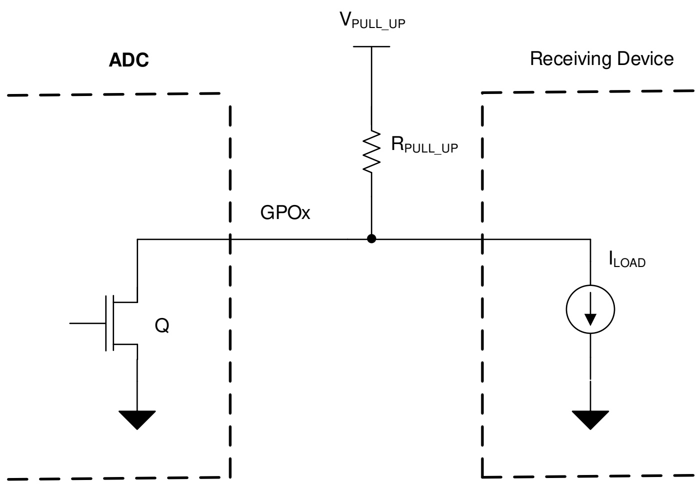


Figure 48. Digital Open-Drain Output

The minimum value of the pullup resistor, as calculated in Equation 3, is given by the ratio of V_{PULL_UP} and the maximum current supported by the device digital output (5 mA).

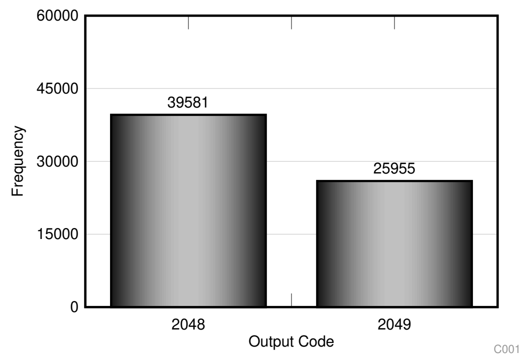
$$R_{MIN} = (V_{PULL\_UP} / 5\ mA) \quad (3)$$

The maximum value of the pullup resistor, as calculated in Equation 4, depends on the minimum input current requirement, I_{LOAD}, of the receiving device driven by this GPIO.

$$R_{MAX} = (V_{PULL\_UP} / I_{LOAD}) \quad (4)$$

Select R_{PULL_UP} such that $R_{MIN} < R_{PULL\_UP} < R_{MAX}$.

8.2.1.3 Application Curve



Standard deviation = 0.49 LSB

Figure 49. DC Input Histogram

Typical Applications (continued)

8.2.2 Digital Push-Pull Output

The channels of the TLA2528 can be configured as digital push-pull outputs supporting an output voltage up to AVDD. As shown in Figure 50, a push-pull output consists of two mirrored opposite bipolar transistors, Q1 and Q2. The device can both source and sink current because only one transistor is on at a time (either Q2 is on and pulls the output low, or Q1 is on and sets the output high). A push-pull configuration always drives the line opposed to an open-drain output where the line is left floating.

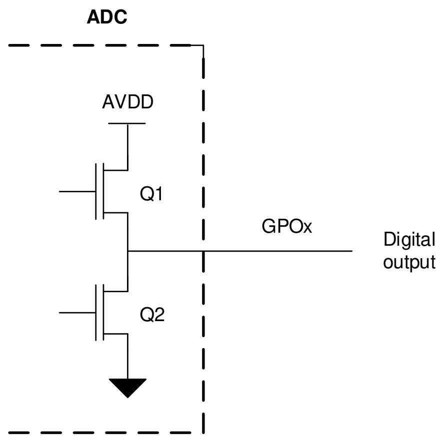


Figure 50. Digital Push-Pull Output

9 Power Supply Recommendations

9.1 AVDD and DVDD Supply Recommendations

The TLA2528 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. For supplies greater than 2.35 V, AVDD and DVDD can be shorted externally if single-supply operation is desired. The AVDD supply also defines the full-scale input range of the device. Decouple the AVDD and DVDD pins individually, as shown in Figure 51, with 1-µF ceramic decoupling capacitors. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

Connect a 1-µF decoupling capacitor between the DECAP and GND pins for the internal power supply.

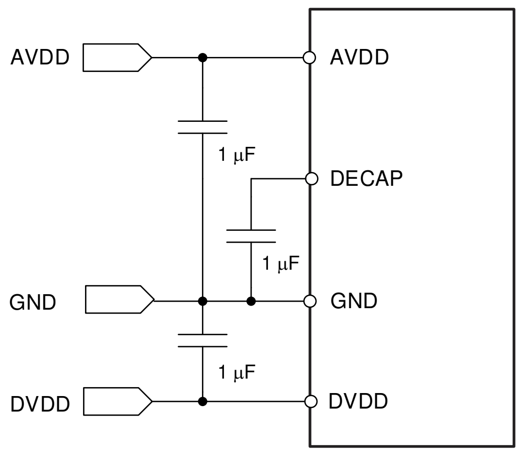


Figure 51. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

Figure 52 shows a board layout example for the TLA2528. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the AVDD supply away from noise sources.

Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect the GND pin to the ground plane using short, low-impedance paths. The AVDD supply voltage also functions as the reference voltage for the TLA2528. Place the decoupling capacitor for AVDD close to the device AVDD and GND pins and connect the decoupling capacitor to the device pins with thick copper tracks.

10.2 Layout Example

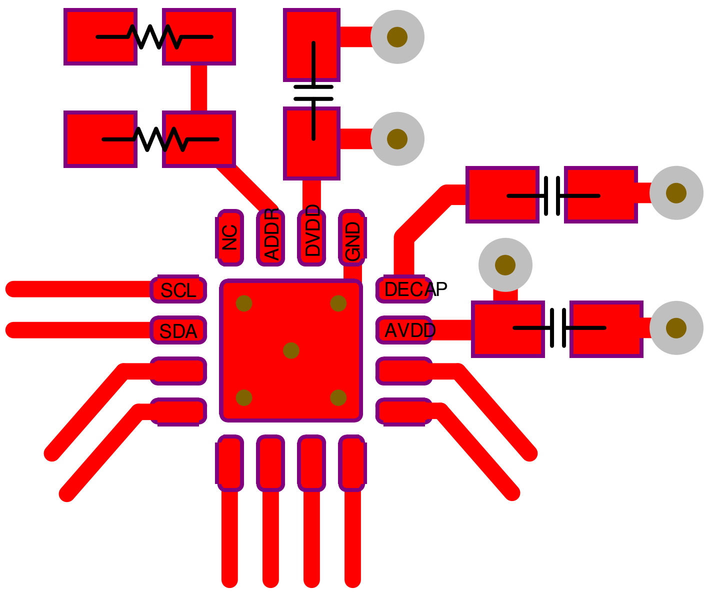


Figure 52. Example Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

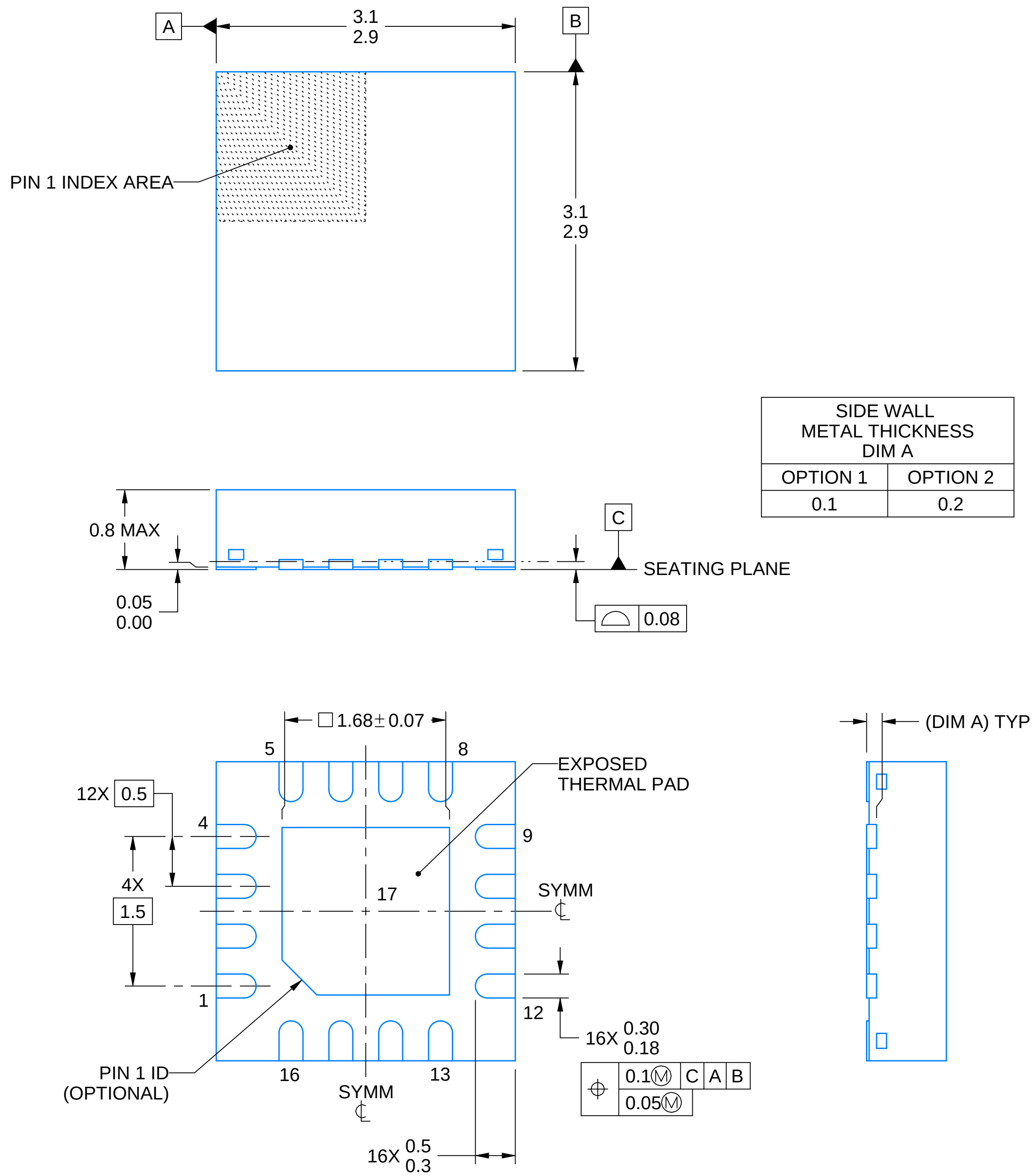
11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

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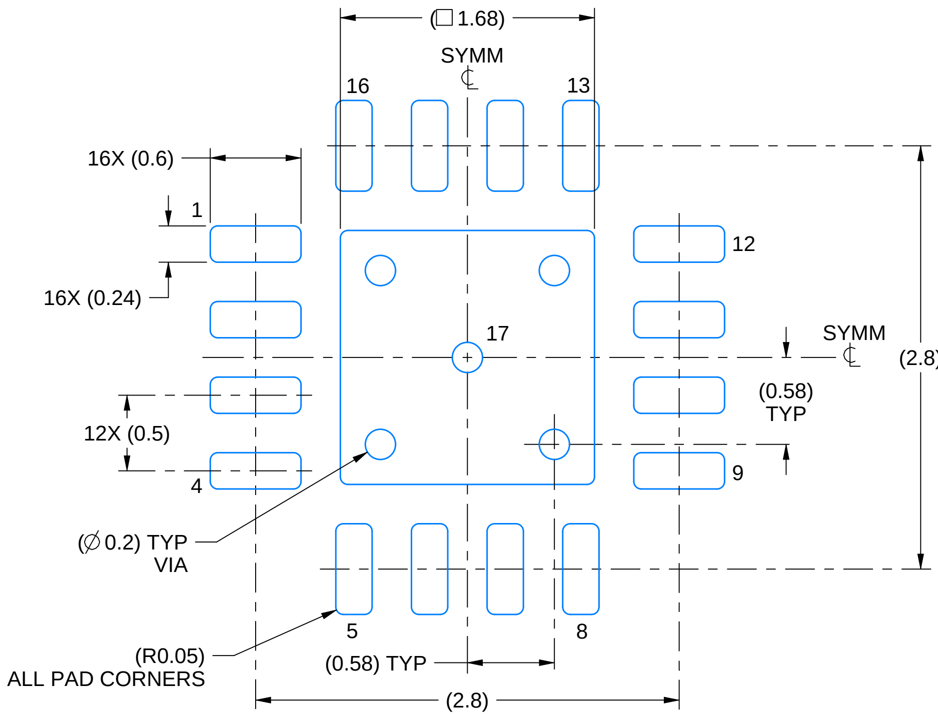
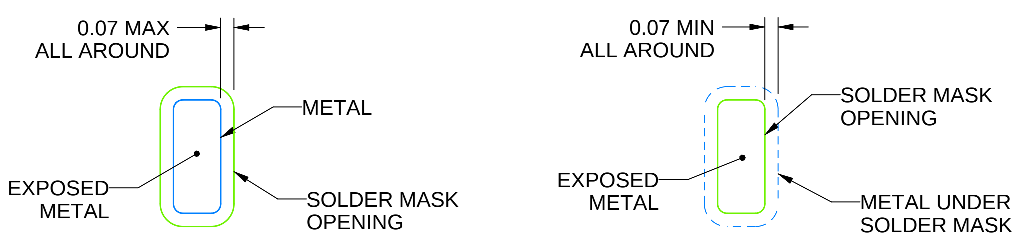
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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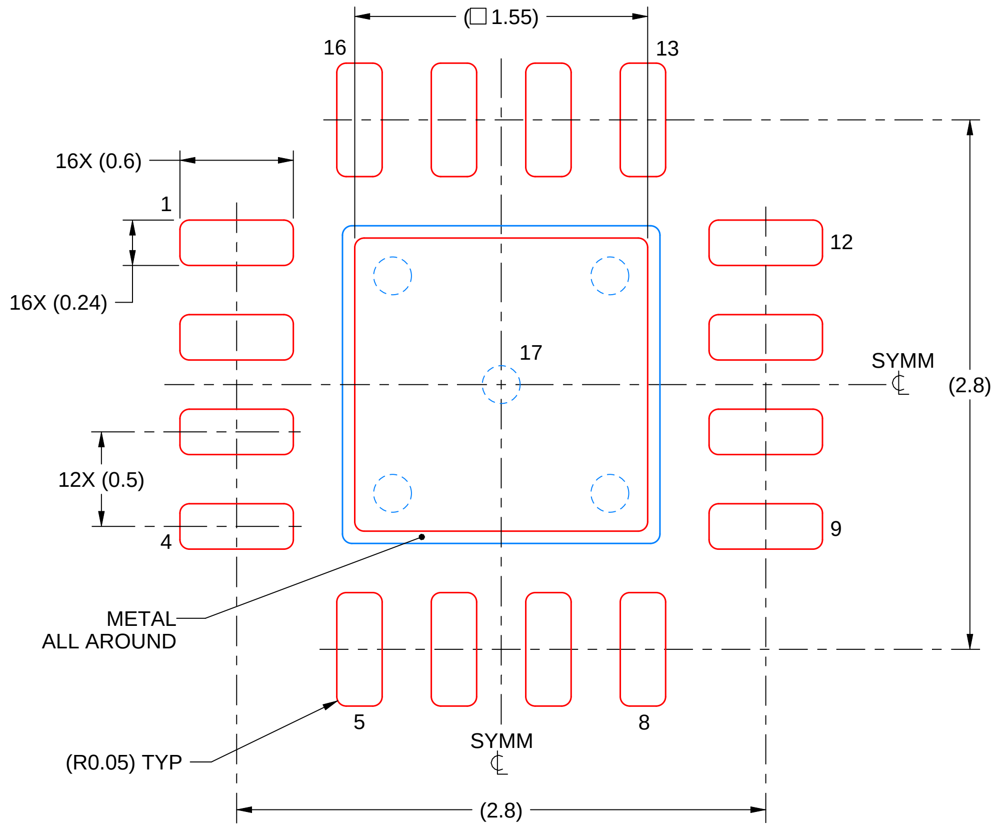
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLA2528IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2528	Samples
TLA2528IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2528	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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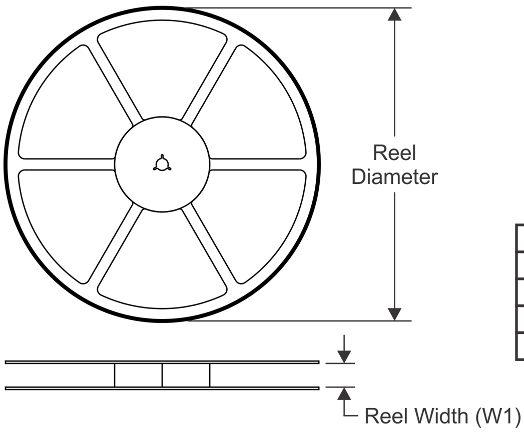
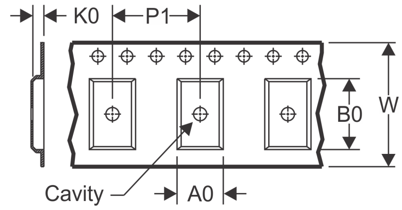
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

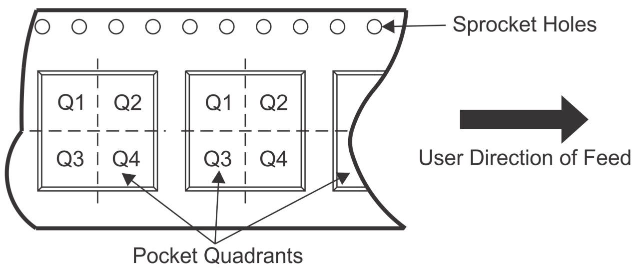


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

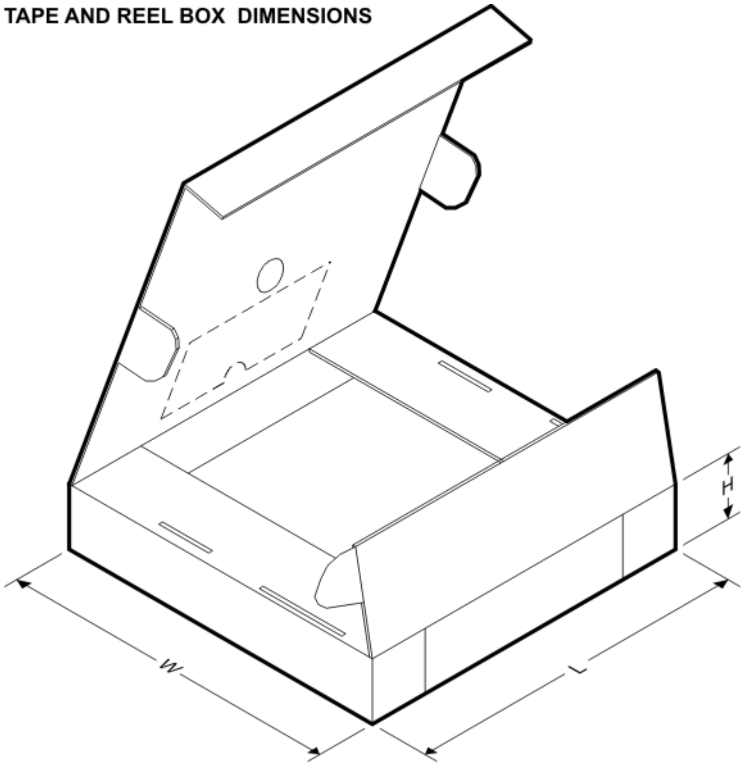
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLA2528IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLA2528IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLA2528IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLA2528IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

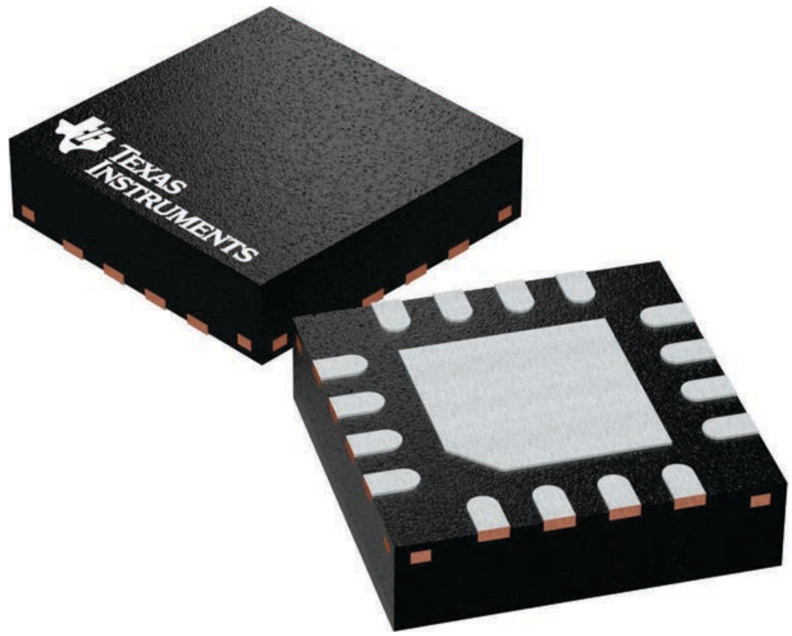
RTE 16

WQFN - 0.8 mm max height

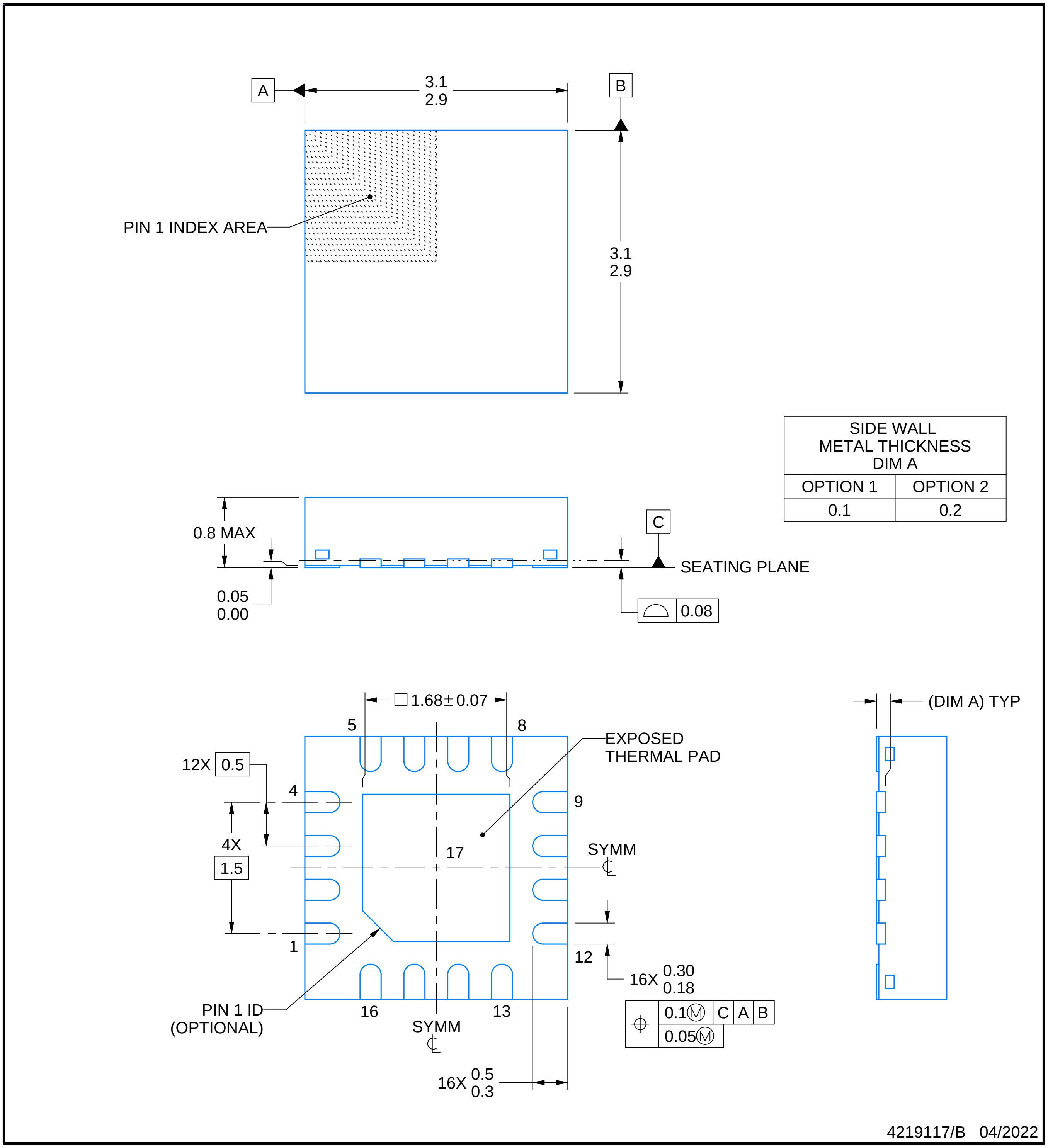
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



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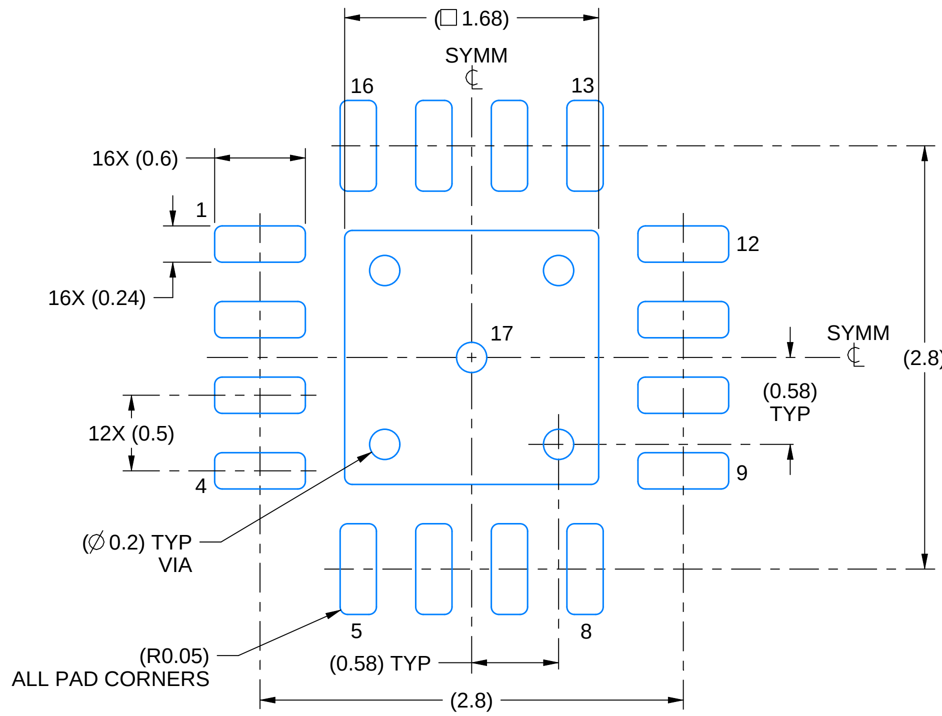
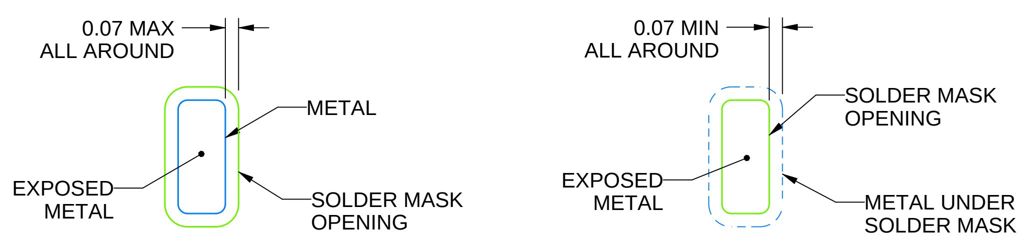


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
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(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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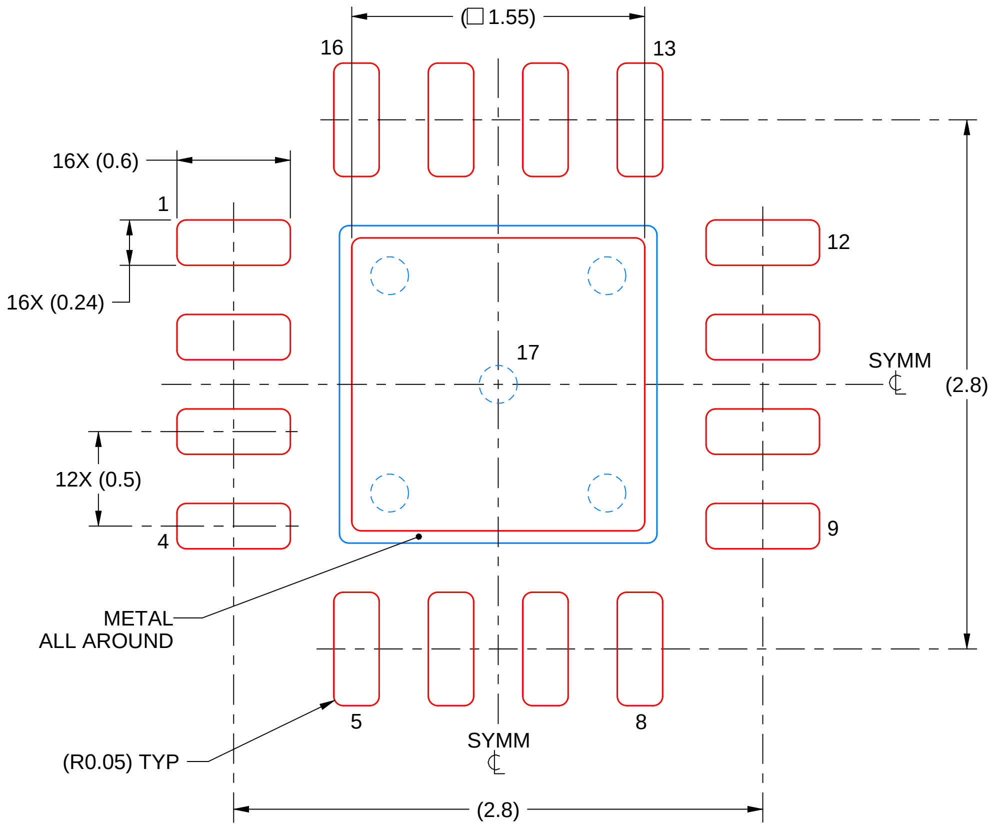

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

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